signetics

TRI-STATE OUTPUT DUAL 50-100-200 BIT STATIC SHIFT REGISTERS

SILICON GATE MOS 2000 SERIES

2509
2510
2511

DESCRIPTION

These Signetics 2500 Series Dual 50, 100, and 200 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals plus TRI-STATE outputs are provided for maximum interfacing capability.

FEATURES

- TRI-STATE MOS OUTPUTS - PROVIDE POWERFUL BUSSING CAPABILITY
- TTL/DTL COMPATIBLE CLOCKS - PROVIDE EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- THREE BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION
- 2MHz GUARANTEED CLOCK RATE
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGES - 10 LEAD TO-100, 14 PIN DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES - LINE STORAGE

SPECIAL FEATURES

The three clock phases used by the register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL 5V logic level input.

The output has three states:
"1" low impedance to +5V
"0" low impedance to -5V
"OFF" high impedance ≃ 10 M ohm
The "OFF" state is controlled by the Output Enable control input.

PROCESS TECHNOLOGY

Use of low threshold silicon gate technology allows high speed (2 MHz Guaranteed) while reducing power dissipation and clock input capacitance dramatically as compared to conventional technologies.

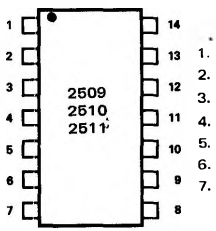
The use of low voltage circuitry minimizes power dissipation and facilitates interfacing with bipolar integrated circuits.

BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits. The TRI-STATE output stage provides driving capability for both MOS and bipolar integrated circuits (one standard TTL load).

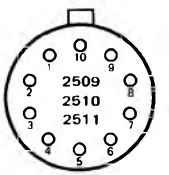
PIN CONFIGURATIONS (Top View)

A PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. NC
5. NC
6. NC
7. V_{DD}
8. ϕIN
9. Output Enable
10. V_{GG}
11. NC
12. OUT_2
13. IN_2
14. V_{CC}

K PACKAGE



1. IN_1
2. OUT_1
3. V_{DD}
4. ϕIN
5. V_{CC}
6. Output Enable
7. V_{GG}
8. OUT_2
9. IN_2
10. $\overline{\text{Recirculate}}$

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2509K	Dual 50	10 Pin, TO-100
2509A	Dual 50	14 Pin, DIP
2510K	Dual 100	10 Pin, TO-100
2510A	Dual 100	14 Pin, DIP
2511K	Dual 200	10 Pin, TO-100
2511A	Dual 200	14 Pin, DIP

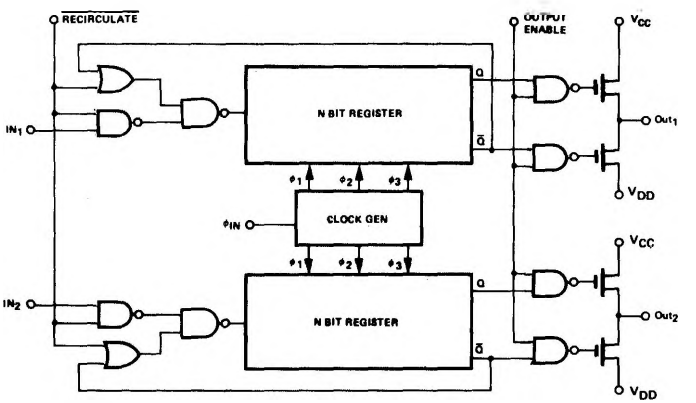
MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation (A & K) (Note 2) @ T_A = 70°C	535mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC} (3)	+0.3V to -20V

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless otherwise specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}. V_{IH} and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

BLOCK DIAGRAM



NOTES:
1: If output enable = "0", output is "off".
2: If output enable = "1", see Truth Table.

TRUTH TABLE:

$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

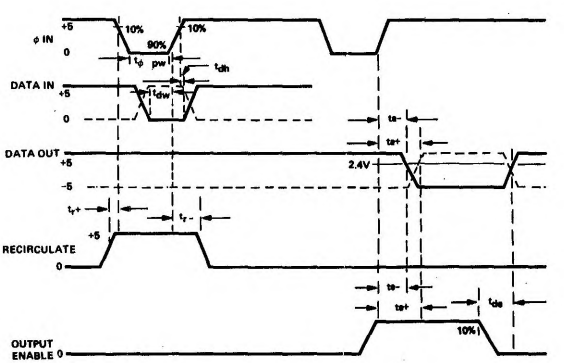
NOTE: "0" = OV; "1" = +5V.

DC CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = +5V (8), V_{DD} = -5V ±5%; V_{GG} = -12V ±5% unless otherwise noted. (Notes 4,5,6,7)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} =-5.5V, T_A = 25°C
I_{LO}	Output Leakage Current		10	1000	nA	V_{CE} =1.05V,T_A = 25°C, V_{OUT} = -5V
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{DD}	Power Supply Current					
	(Dual 50)		6.5	15	mA	Continuous Operation
	(Dual 100)		12	30	mA	F = 2MHz, T_A = 25°C
	(Dual 200)		20	40	mA	
I_{GG}	Power Supply Current		4.5	7.5	mA	
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage	-5		1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

TIMING DIAGRAM

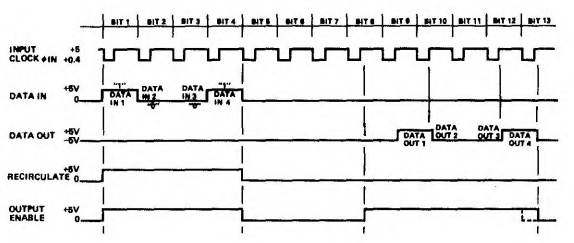


AC CHARACTERISTICS

V_{CC} = +5V (8); V_{DD} = -5V ±5%; V_{ILC} = +0.4V to 4V; V_{GG} = -12V ±5%; T_A = 0° C to +70°C

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	DC	3	1.5	MHz	
t_{ϕ} PW	Clock Pulse Width	.290	.150	100	μsec	
$\overline{t_{\phi}\ PW}$	Clock Pulse Width	.210		DC	μsec	
t_r; t_f	Clock Pulse Transition			1	μsec	
t_{DW}	Data Write (Set-up) Time	50			nsec	
t_{DH}	Data to Clock Hold Time	50			nsec	
t_{a+}; t_{a-}	Clock to Data Out Delay		200	350	nsec	
t_a+; t_a−	Clock to Data Out Delay			500	nsec	I_{OL} = O, I_{OL} = 1.6mA
t_{cs}−, t_{cs}+	Output Enable to Data Out			300	nsec	
t_{DE}	Output Enable to Data Out Disconnect			300	nsec	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_{OUT}	Output Capacitance			5	pF	@ 1 MHz; V_{OUT} = V_{CC}; V_{AC} = 25mV p-p
C_{ϕ}	Clock Capacitance			5	pF	@ 1 MHz; V_{ϕ} = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load I_L = 1.6mA
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	3.0	3.5		V	1 TTL load (I_L = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	3.6	4		V	

TIMING DIAGRAM



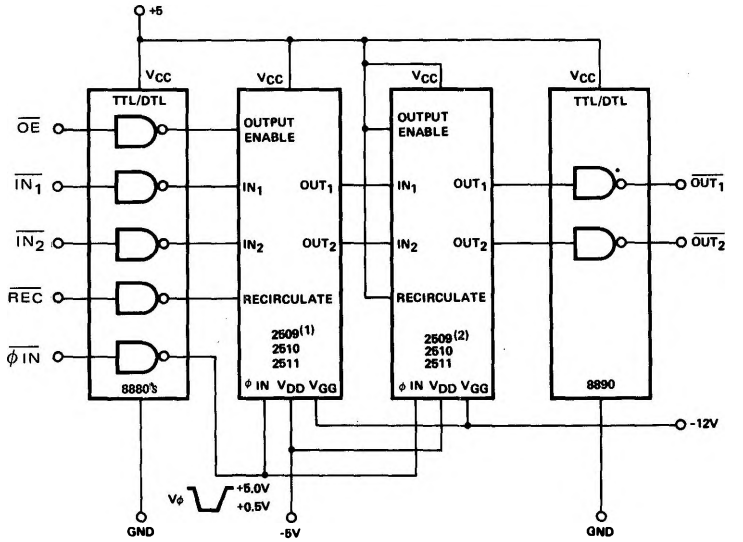
NOTE 1: WRITE CYCLE
The positive going edge of the recirculate control is coincident with the negative going edge of the input clock (ϕ_{IN}). The output enable control may be either "1" or "0".

NOTE 2: RECIRCULATE CYCLE
Data recirculates if the recirculate control is a "0" the output enable may be either "1" or "0".

NOTE 3: READ CYCLE
The negative going edge of the output enable control is coincident with the positive edge of the clock (ϕ_{IN}). Recirculate may be either "1" or "0".

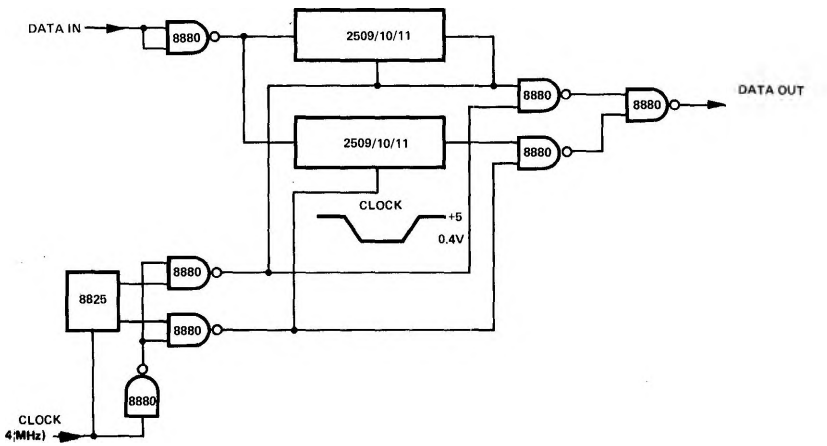
APPLICATIONS INFORMATION

TTL/DTL/MOS INTERFACES



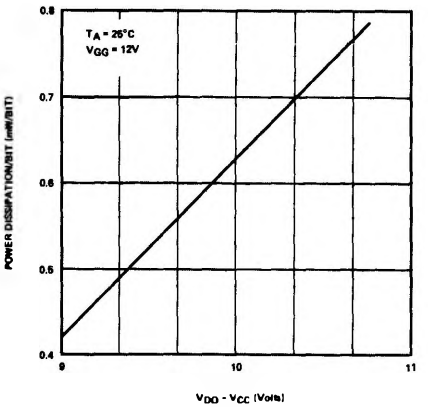
NOTES:
1. Register used as a recirculating register.
2. Register used as serial in/serial out shift register.

MULTIPLEXING MEMORY REGISTERS AT 4MHz DATA RATE

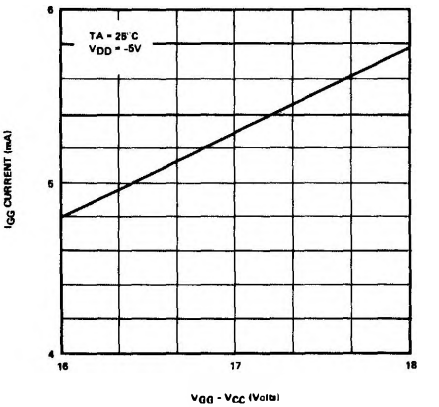


CHARACTERISTIC CURVES

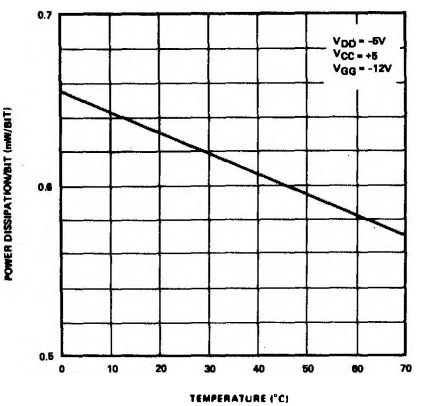
POWER DISSIPATION/BIT VERSUS V_{DD} SUPPLY VOLTAGE



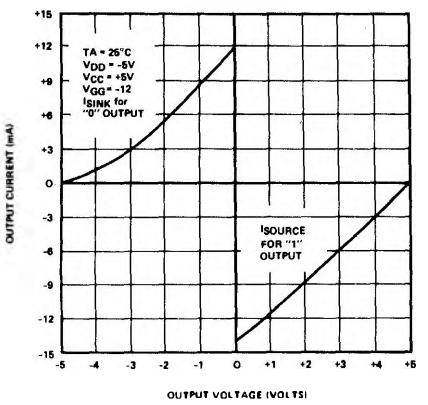
I_{GG} CURRENT VERSUS V_{GG} SUPPLY VOLTAGE



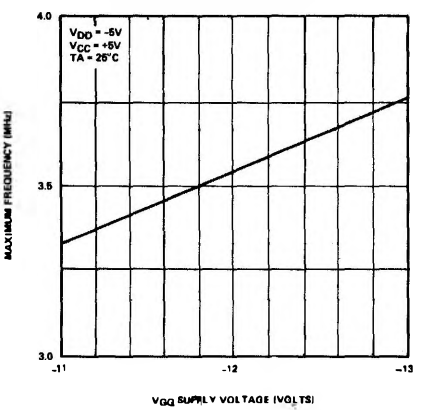
POWER DISSIPATION/BIT VERSUS TEMPERATURE



OUTPUT VOLTAGE VERSUS OUTPUT CURRENT

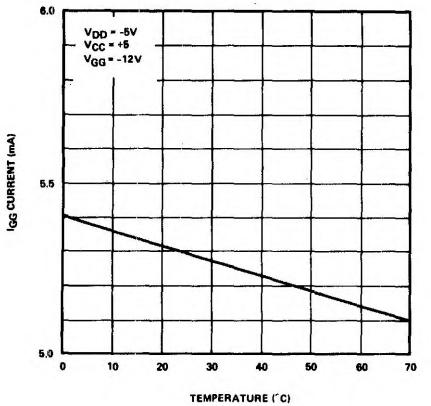


MAXIMUM FREQUENCY VERSUS V_{GG} SUPPLY VOLTAGE

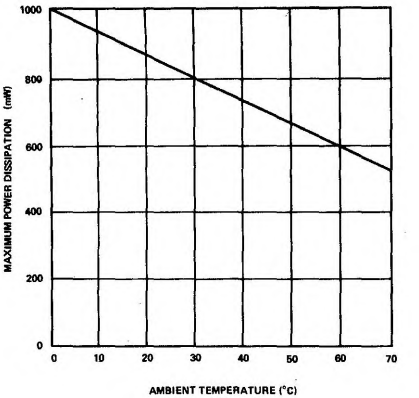


CHARACTERISTIC CURVES (Cont'd.)

I_{GG} CURRENT VERSUS TEMPERATURE



PACKAGE MAXIMUM POWER DISSIPATION



SCHEMATIC DIAGRAM