signetics

DUAL 128-132 BIT STATIC SHIFT REGISTERS

2521
2522

SILICON GATE MOS 2500 SERIES

DESCRIPTION

These Signetics 2500 Series Dual 128 and 132 bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip.

FEATURES

- PUSH-PULL OUTPUTS
- TTL/DTL COMPATIBLE CLOCK – PROVIDES EXTREMELY LOW CLOCK CAPACITANCE
- RECIRCULATION PATH ON CHIP
- TWO BIT LENGTHS AVAILABLE
- HIGH FREQUENCY OPERATION – 2MHz TYPICAL CLOCK RATE
- TTL, DTL COMPATIBLE SIGNALS
- STANDARD PACKAGE – 8 LEAD SILICONE DIP
- SIGNETICS P-MOS SILICON GATE PROCESS TECHNOLOGY

APPLICATIONS

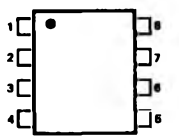
LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
LINE PRINTERS
CASSETTE RECORDERS

BIPOLAR COMPATIBILITY

The clock and signal inputs of these registers can be driven directly by standard bipolar integrated (TTL, DTL, etc.) or by MOS circuits.

PIN CONFIGURATION (Top View)

V PACKAGE



1. $\overline{\text{Recirculate}}$
2. IN_1
3. OUT_1
4. V_{GG}
5. ϕ_{IN}
6. OUT_2
7. IN_2
8. V_{CC}

TRUTH TABLE

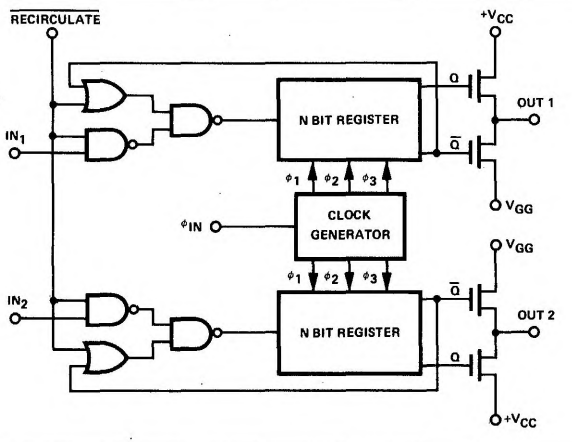
$\overline{\text{RECIRCULATE}}$	INPUT	FUNCTION
0	0	Recirculate
0	1	Recirculate
1	0	"0" is Written
1	1	"1" is Written

NOTE: "0" = 0V; "1" = +5V.

PART IDENTIFICATION TABLE

PART NUMBER	BIT LENGTH	PACKAGE
2521V	Dual 128	8 Pin DIP
2522V	Dual 132	8 Pin DIP

BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C
Storage Temperature	-65°C to +150°C
Package Power Dissipation at T_A = 70°C	535 mW
Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V

NOTES:

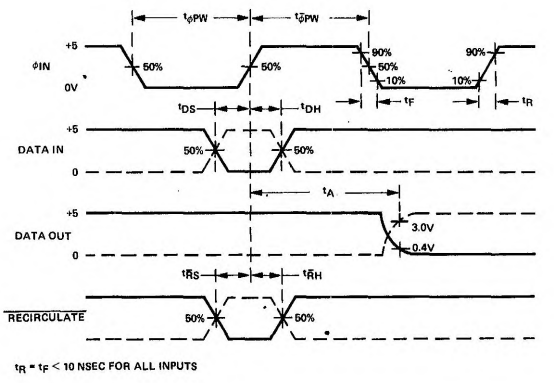
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserving the right to make design and process changes and improvements.
7. Typical values are at +25°C and nomin. supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	INPUT LOAD CURRENT		10	500	nA	V_{in} = 5.5V, T_A = 25°C
I_{LC}	CLOCK LEAKAGE CURRENT		10	500	nA	V_{ILC} = GND, T_A = 25°C
I_{GG}	POWER SUPPLY CURRENT		28	32	mA	CONTINUOUS OPERATION F = 1.5MHz, T_A=25°C
V_{IL}	INPUT "LOW" VOLTAGE			1.05	V	
V_{IH}	INPUT "HIGH" VOLTAGE	3.2		5.3	V	
V_{ILC}	CLOCK INPUT "LOW" VOLTAGE			1.05	V	
V_{IHC}	CLOCK INPUT "HIGH" VOLTAGE	3.2		5.3	V	

CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL gate

TIMING DIAGRAM



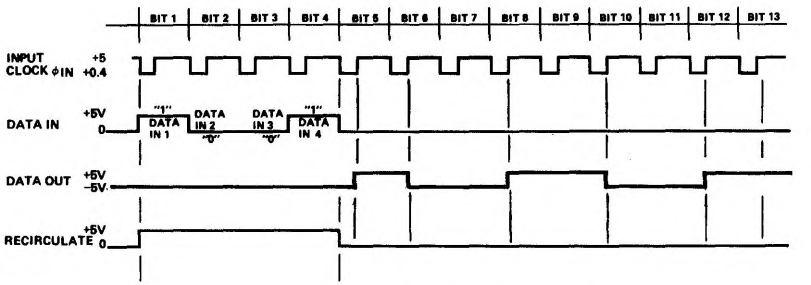
$t_R = t_F < 10$ NSEC FOR ALL INPUTS

AC CHARACTERISTICS V_{CC} = +5V (8); V_{GG} = -12V ±5%, V_{IC} = 0.4 to 4.0; T_A=0° to +70°C

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
FREQUENCY	CLOCK REP RATE	DC		1.5	MHz	See Maximum Frequency Curve
$t_{\phi PW}$	CLOCK PULSE WIDTH	.350	.100	100	μsec	
$t_{\overline{\phi} PW}$	$\overline{\text{CLOCK}}$ PULSE WIDTH	.200		DC	μsec	
t_R, t_F	CLOCK PULSE TRANSITION			1	usec	
t_{DS}	DATA WRITE (SET-UP) TIME	75			nsec	
t_{DH}	DATA TO CLOCK HOLD TIME	50			nsec	
t_A	CLOCK TO DATA OUT DELAY		250	350	nsec	
$t_{\overline{RS}}$	$\overline{\text{RECIRCULATE}}$ SET-UP TIME	50			ns	
$t_{\overline{RH}}$	$\overline{\text{RECIRCULATE}}$ HOLD TIME	50			ns	
C_{IN}	INPUT CAPACITANCE			5	pF	@ 1MHz; $V_{in} = V_{CC}$; V_{AC} = 25mV p-p
$C\phi$	CLOCK CAPACITANCE			5	pF	@ 1MHz; $V_\phi = V_{CC}$; V_{AC} = 25mV p-p
V_{OL}	OUTPUT "LOW" VOLTAGE	-4.0		0.4	V	1 TTL load (I_L=1.6mA)
V_{OH1}	OUTPUT "HIGH" VOLTAGE DRIVING 1 TTL LOAD	3.0	3.5		V	1 TTL load (I_I = 100μA)
V_{OH2}	OUTPUT "HIGH" VOLTAGE DRIVING MOS	3.5	4.0		V	

TIMING DIAGRAM

4 BIT RECIRCULATING SHIFT REGISTER *

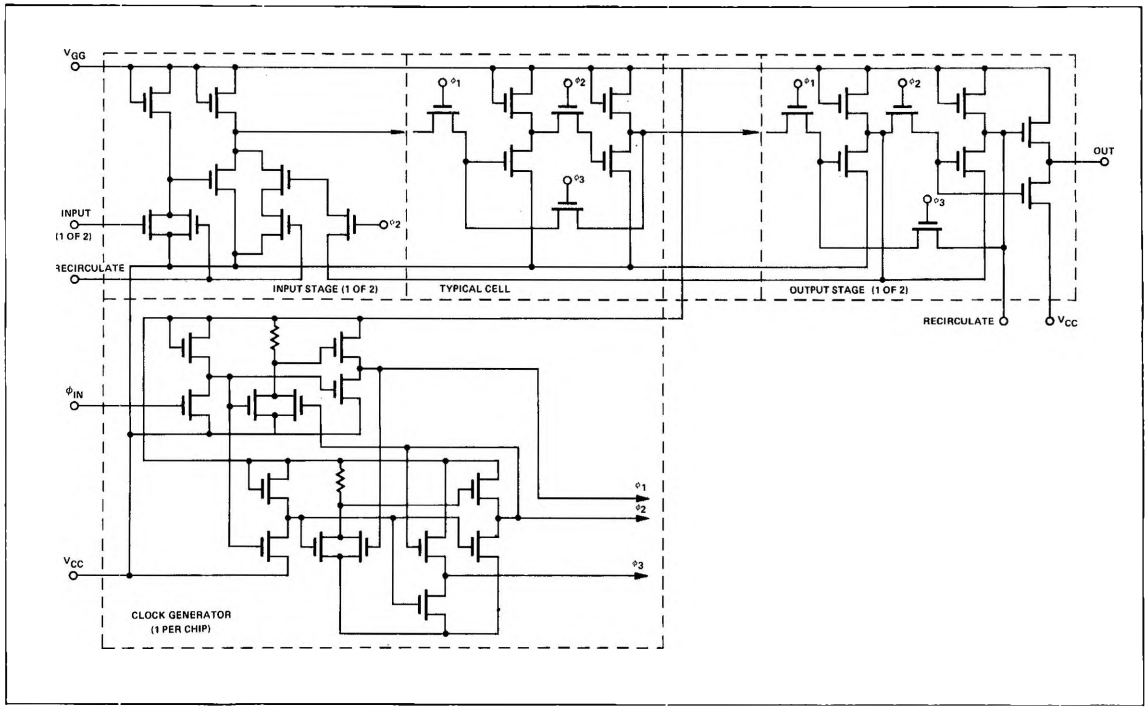


NOTE 1: WRITE CYCLE
The positive going edge of the recirculative control is coincident with the negative going edge of the input clock (ϕ_{IN}).

NOTE 2: RECIRCULATE CYCLE
Data recirculates if the recirculate control is a "0"

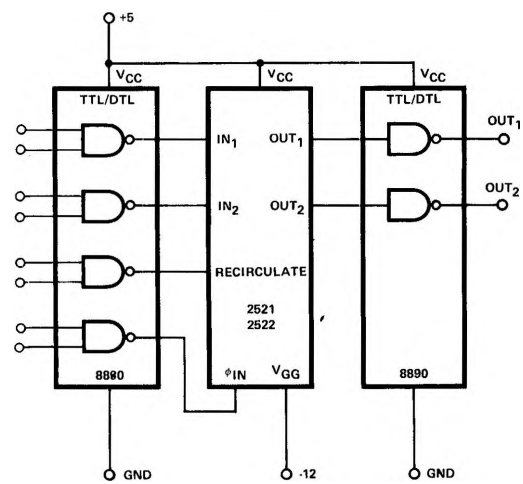
*For clarity, a four bit hypothetical example is shown

SCHEMATIC DIAGRAM



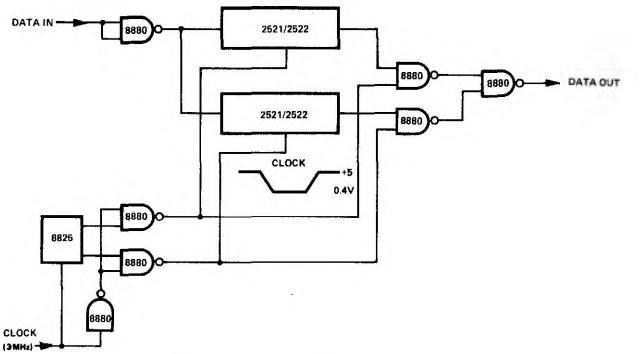
APPLICATIONS DATA

TTL/DTL/MOS INTERFACES



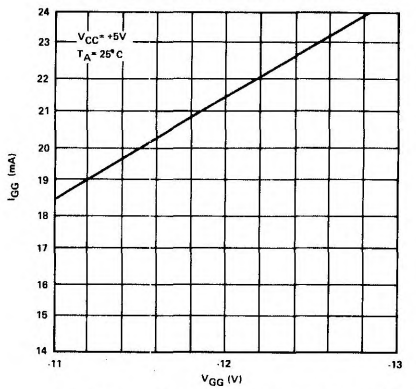
APPLICATIONS INFORMATION

MULTIPLEXING LINE MEMORY REGISTERS AT 3MHz DATA RATE

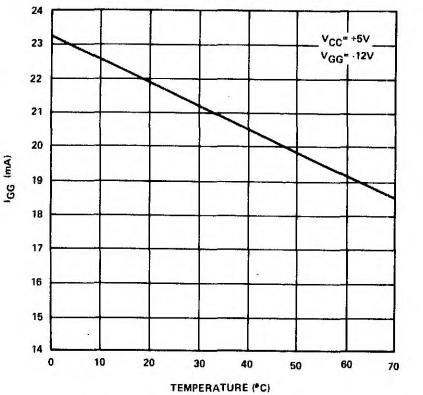


CHARACTERISTIC CURVES

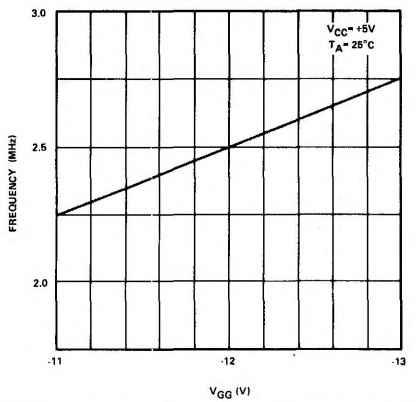
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



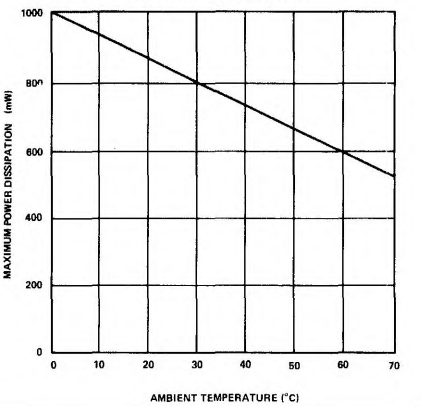
POWER SUPPLY CURRENT VERSUS TEMPERATURE



TYPICAL OPERATING FREQUENCY VERSUS SUPPLY VOLTAGE



PACKAGE MAXIMUM POWER DISSIPATION



132 COLUMN LINE PRINTER