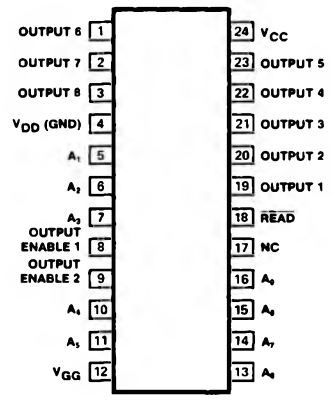
2530-1,N

DESCRIPTION

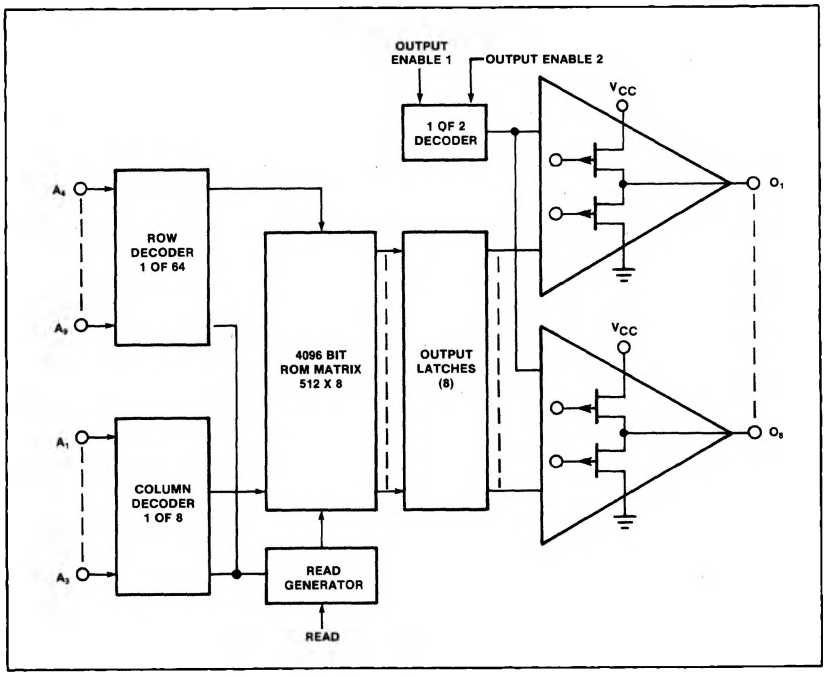
The 2530 has a read input which controls the entry of data from the ROM into output latches. Three-state outputs allow OR-tying for implementing larger memories. Two mask programmable output enables control the 8 output devices without affecting address circuitry.

PIN CONFIGURATION

I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to +150	
P_D	Power dissipation at 70°C[2]	730	mW
	Input and supply voltages with respect to V_{CC}[3]	+0.3 to -20	V

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = 0V, V_{GG} = -12V ± 5%, unless otherwise specified.[4,5,6,7]

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[8]					V
V_{IL}	Low		-5		0.6	
V_{IH}	High		3.4		5.3	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.5	
V_{OH}	High	I_{OH} = 100μA	3.8			
I_{LI}	Input load current	V_{IN} = -5.5V, T_A = 25°C		10	500	nA
I_{LO}	Output leakage current	V_{OUT} = 0V, T_A = 25°C		10	1000	nA
	Supply current[9]					mA
I_{CC}	V_{CC}			30	45	
I_{GG}	V_{GG}			30	45	
C_{IN}	Address input capacitance	V_{IN} = V_{CC}, V_{AC} = 25m p-p, f=1MHz			10	pF

AC ELECTRICAL CHARACTERISTICS

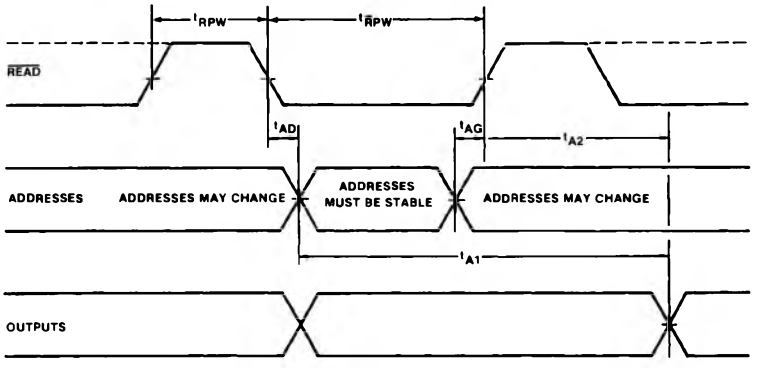
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{DD} = 0V, V_{GG} = -12V ± 5%, unless otherwise specified.

PARAMETER		TO	FROM	LIMITS			UNIT
				Min	Typ	Max	
	Pulse width						ns
t_{RPW}	$\overline{\text{Read}}$[10]			250	200		
$t_{\overline{RPW}}$	$\overline{\text{Read}}$[11]			500	400		
	Address time[12]						ns
t_{AD}	Delay	Address	$\overline{\text{Read}}$ low			50	
t_{AG}	Read	$\overline{\text{Read}}$ high	Address			50	
	Delay time						ns
t_{A1}[13]		Output	Address		625	700	
t_{A2}[13]		Output	End of read pulse		200	250	
t_{OE}		Output	Output enable		100	250	

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on +150°C maximum junction temperature and a thermal resistance of 110°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and typical supply voltages.
8. Guaranteed input levels are stated for worst case conditions including a ±5% variation in V_{CC} and a temperature variation of 0°C to 70°C. Actual input requirements with respect to V_{CC} are V_{IH} = V_{CC} -1.85V and V_{IL} = V_{CC} -4.15V.
9. Outputs open, t_{RPW} = 250ns, $t_{\overline{RPW}}$ = 500ns.
10. During $t_{\overline{RPW}1}$ addresses are decoded and sent to the memory matrix and the stored memory data is moved to the data inputs of the output RS latches. This data is clocked into the output latches at the end (rising edge) of the $\overline{\text{read}}$ pulse. After t_{A2} data appears at the output terminals.
11. During t_{RPW1} data is clocked into the output latches and the address decoders are precharged in preparation for the next cycle.
12. Addresses must be stable within 50ns after the $\overline{\text{read}}$ line falls and must remain stable until at least 50ns before the $\overline{\text{read}}$ line goes high.
13. t_A = 0°C to +70°C.

TIMING DIAGRAM



All times measured from 50% points, for all input waveforms $t_r = t_f = 10ns$.

CUSTOM CODING INFORMATION

Data Card Format

HEADER CARD

Card No. 1

Columns	
1-5	2530N or 25301
6-14	Blank
15-19	CODED
20	Blank
21	Logic state of Output Enable #2, (CS2)-Most Significant Bit
22	Logic state of Output Enable #1
23	Blank
24-71	Customer company name
72	Blank
73-80	Date

I.D./ COMMENT CARDS

Card No. 1

Columns	
1	C
2	Blank
3-80	Person responsible for reviewing Signetics truth table and company name

Card No. 2

Columns	
1	C
2	Blank
3-80	Customer city, state, zip

DATA CARDS

Card No. 1

Columns	
1-3	Decimal address (blank, blank, 0)
4	Blank
5-12	8-digit binary output (MSB-left)*
13-20	Blank
21-33	Decimal address (blank, blank, 1)
24	Blank
25-32	8-digit binary output (MSB-left)*
33-40	Blank
41-43	Decimal address (blank, blank, 2)
44	Blank
45-52	8-digit binary output (MSB-left)*
53-60	Blank
61-63	Decimal address (blank, blank, 3)
64	Blank
65-72	8-digit binary output (MSB-left)*
73-80	Blank

Card No. 2

Same format as Card No. 1

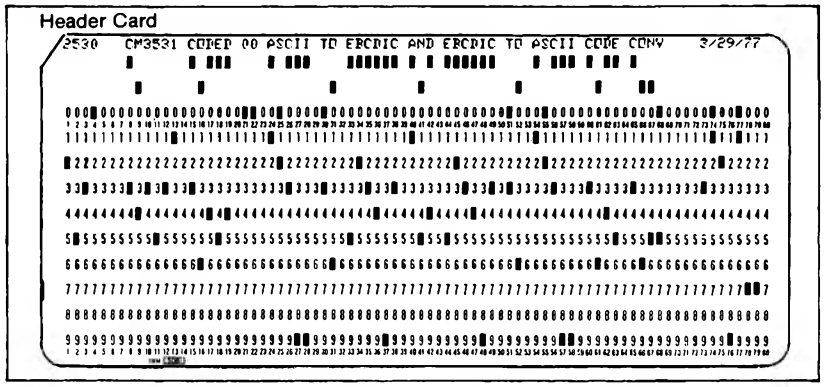
Card No. 128

128 Same format as Card No. 1

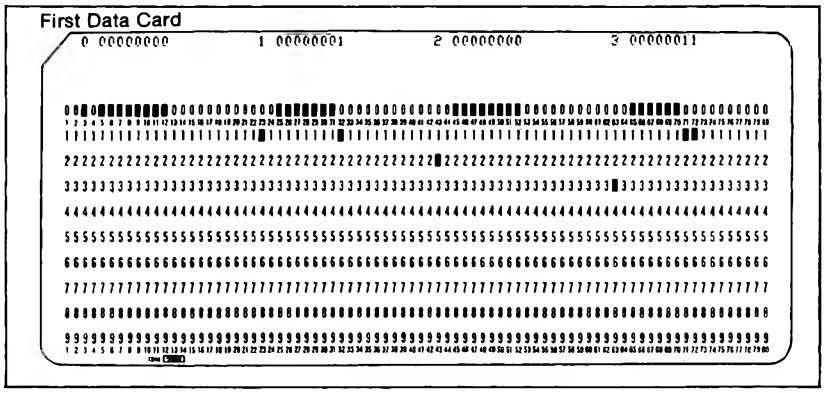
*MSB = O_8

EXAMPLES

Header Card



First Data Card



Last Data Card