signetics

QUAD 80-BIT STATIC SHIFT REGISTER | 2532

SILICON GATE MOS 2500 SERIES

DESCRIPTION

The Signetics 2532 Static Shift Register consists of enhancement mode P-Channel silicon gate MOS devices integrated on a single monolithic chip. Each of the four 80-bit registers is provided with an independent input, push-pull output and recirculation control. The single phase clock is common to all four registers. All inputs and outputs including the clock interface directly with TTL or DTL circuits without external components.

Data is entered when the clock is at a logic "1". Data is shifted when the clock goes low. When the Recirculate control is at a logic "1", data recirculates and is continuously available at the output, data input is inhibited. With the Recirculate control is at a logic "0", data is entered.

FEATURES

- TOTAL TTL COMPATIBILITY
- SINGLE CLOCK LINE
- RECIRCULATE PATH ON CHIP
- DC TO 2.5 MHz OPERATION GUARANTEED
- LOW POWER (TYPICALLY 400 μW/BIT)
- PIN-FOR-PIN REPLACEMENT FOR (DYNAMIC) MK1007P AND TMS3409
- POWER SUPPLIES +5V AND −12V

APPLICATIONS

LOW COST SEQUENTIAL ACCESS MEMORIES
LOW COST STATIC BUFFER MEMORIES
CRT REFRESH MEMORIES – LINE STORAGE
DELAY LINES
DIGITAL FILTERING

SPECIAL FEATURES

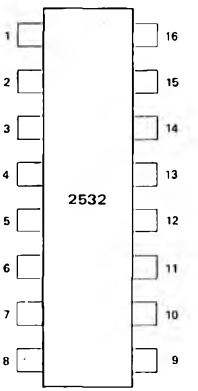
The three clock phases used by the static register cells are generated internally by an on-chip generator. This clock generator is controlled by a single TTL/DTL logic level input.

BIPOLAR COMPATIBILITY

All inputs of these registers, including the clock can be driven directly by bipolar TTL/DTL integrated circuits without external components. Outputs are push-pull operating between 0V and +5V and provide a sink current of 1.6mA for one TTL fanout.

PIN CONFIGURATION (Top View)

B PACKAGE



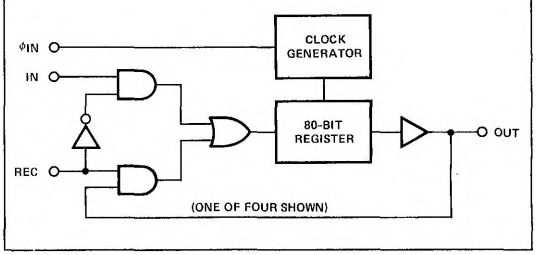
1.	OUT 1	16.	V_{CC}
2.	Recirculate 1	15.	IN 4
3.	IN 1	14.	Recirculate 4
4.	OUT 2	13.	OUT 4
5.	Recirculate 2	12.	V_{GG}
6.	IN 2	11.	ϕ IN
7.	OUT 3	10.	IN 3
8.	V_{DD} (Ground)	9.	Recirculate 3

TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
0	0	"0" is Written
0	1	"1" is Written
1	0	Recirculate
1	1	Recirculate

NOTE: "0" = 0V, "1" = +5V

BLOCK DIAGRAM



PART IDENTIFICATION

PART NUMBER	BIT LENGTH	PACKAGE
2532B	Quad 80	16-Pin DIP

MAXIMUM GUARANTEED RATINGS (1)

Operating Ambient Temperature (2)	0°C to +70°C	Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.3V to -20V
Storage Temperature	-65°C to +150°C		
Package Power Dissipation at T_A = 70°C	640 mW		

DC CHARACTERISTICS T_A = 0°C to +70°C; V_{CC} = +5V(8); V_{GG} = -12V ±5% unless otherwise noted.

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
I_{LI}	Input Load Current		10	500	nA	V_{IN} = 5.5V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	500	nA	V_{ILC} = 0V, T_A = 25°C
I_{GG}	Power Supply Current		6	10	mA	Continuous Operation F = 2.5 MHz, T_A = 25°C Outputs Open
I_{CC}	Power Supply Current		12	20	mA	
V_{IL}	Input "Low" Voltage			1.05	V	
V_{IH}	Input "High" Voltage	3.2		5.3	V	
V_{ILC}	Clock Input "Low" Voltage			1.05	V	
V_{IHC}	Clock Input "High" Voltage	3.2		5.3	V	

AC CHARACTERISTICS T_A = 0°C to 70°C; V_{CC} = +5V(8); V_{GG} = -12V + 5%, V_{IC} = 0.4 to 4.0V

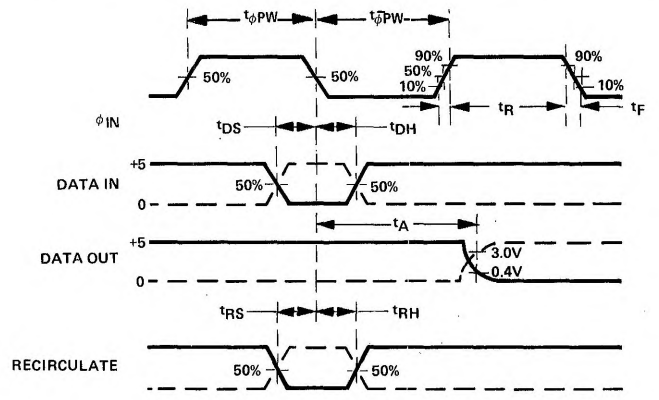
(CONDITIONS OF TEST Input rise and fall times: 10 nsec. Output load is 1 TTL Gate.)

SYMBOL	TEST	MIN	TYP	MAX	UNIT	CONDITIONS
Frequency	Clock Rep Rate	DC	3.0	1.5	MHz	
$t_{\phi PW}$	Clock Pulse Width	0.18		100	μs	
$t_{\overline{\phi}PW}$	Clock Pulse Width	0.22		DC	μs	
t_R,t_F	Clock Pulse Transition			5	μs	
t_{DS}	Data Set-up Time	120			ns	
t_{DH}	Data Hold Time	0			ns	
t_A	Clock to Data Out Delay			400	ns	I_{OL} = 1.6mA
t_{RS}	Recirculate Set-up Time	150			ns	
t_{RH}	Recirculate Hold Time	0			ns	
C_{IN}	Input Capacitance			5	pF	@ 1 MHz; V_{IN} = V_{CC}; V_{AC} = 25mV p-p
C_ϕ	Clock Capacitance			5	pF	@ 1 MHz; V_ϕ = V_{CC}; V_{AC} = 25mV p-p
V_{OL}	Output "Low" Voltage			0.4	V	1 TTL load (I_L = 1.6mA)
V_{OH1}	Output "High" Voltage Driving 1 TTL Load	4.0			V	1 TTL load (I_I = 100μA)
V_{OH2}	Output "High" Voltage Driving MOS	4.0			V	

NOTES:

1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 125°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. V_{CC} tolerance is ±5%. Any variation in actual V_{CC} will be tracked directly by V_{IL}, V_{IH}, and V_{OH} which are stated for a V_{CC} of exactly 5 volts.

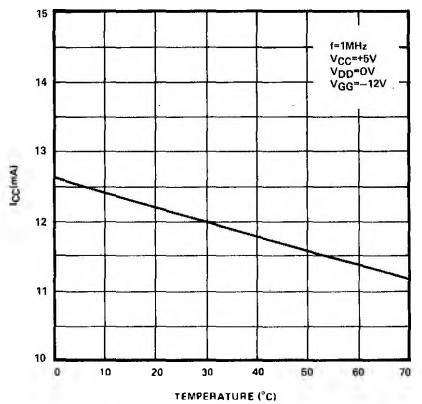
TIMING DIAGRAM



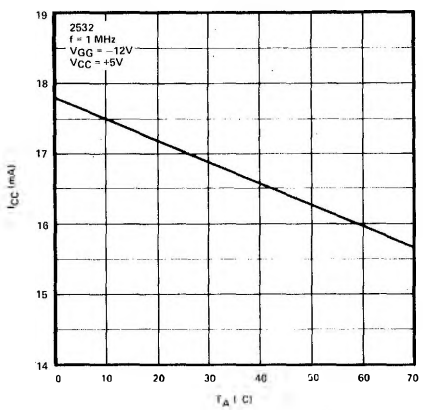
$t_R = t_F < 10$ NSEC FOR ALL INPUTS

CHARACTERISTIC CURVES

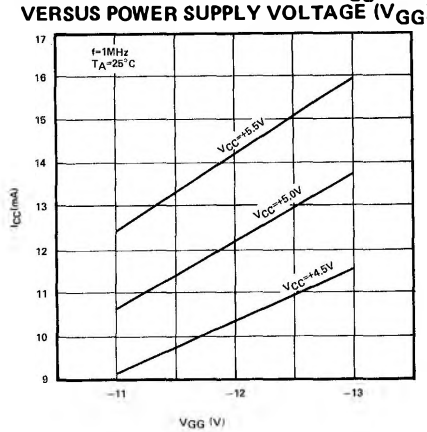
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



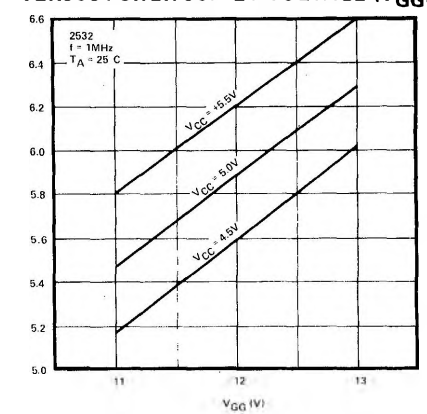
POWER SUPPLY CURRENT (I_{CC}) VERSUS TEMPERATURE



POWER SUPPLY CURRENT (I_{CC}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})

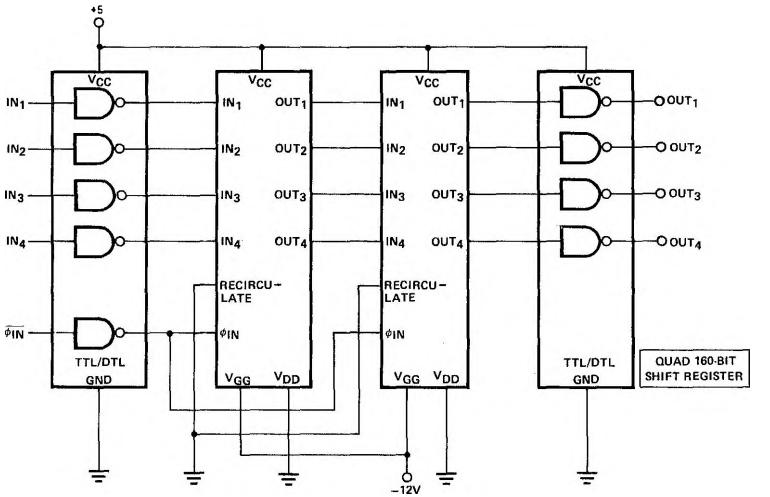


POWER SUPPLY CURRENT (I_{GG}) VERSUS POWER SUPPLY VOLTAGE (V_{GG})



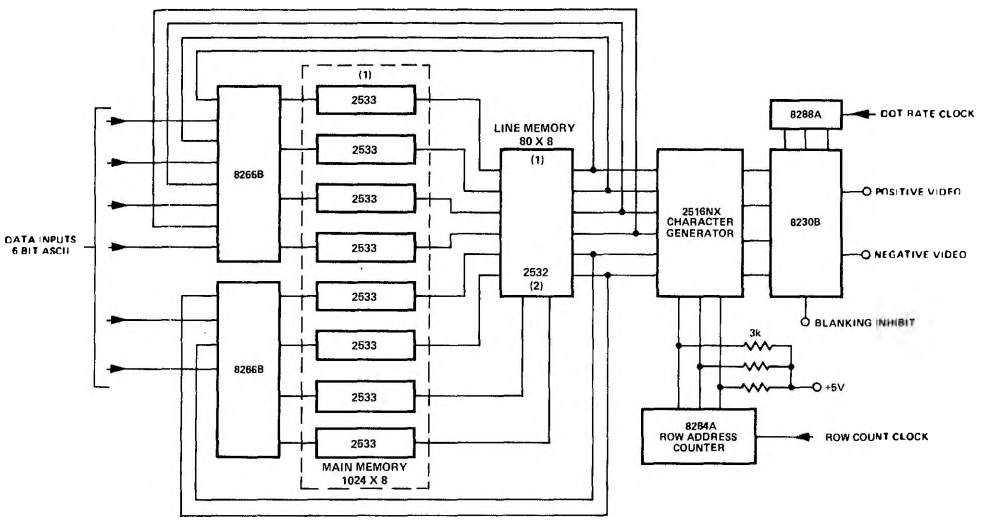
APPLICATIONS INFORMATION

DTL/TTL – MOS – MOS – DTL/TTL INTERFACING



NOTE: All unused inputs must be tied to a "1" or a "0", i.e., MOS inputs cannot be left floating.

12 LINE, 80 CHARACTER PER LINE CRT DISPLAY MEMORY SYSTEM



(1) These registers include internal recirculate. Two 8266B multiplexers are used for system recirculate.