# signetics

# UNIVERSAL ASYNCHRONOUS FIRST-IN, FIRST-OUT BUFFER REGISTER 2535

PRELIMINARY SPECIFICATION

SILICON GATE MOS 2500 SERIES

## DESCRIPTION

The Signetics 2535 is a P-Channel MOS asynchronous buffer memory consisting of 32 8-bit words. Both input and output can be either serial or parallel with a data rate of DC to 1 MHz in either mode of operation.

The register is designed so that information entered at the input will "fall through" to the lowest unoccupied location. Input and output may be accessed asynchronously. Control logic provides flag signals indicating presence of data and availability status of empty storage locations.

The 2535 may be expanded in either the bit or word direction. All inputs and outputs are directly DTL/TTL compatible.

## FEATURES

- ASYNCHRONOUS LOAD AND DUMP
- 32 WORD BY 8-BIT ELASTIC STORAGE
- DC TO 1 MHz OPERATION
- SERIAL OR PARALLEL OPERATION
- TTL COMPATIBLE
- 28-PIN DIP PACKAGE
- $V_{CC}$ = +5 V, $V_{GG}$ = −12 V

## APPLICATIONS

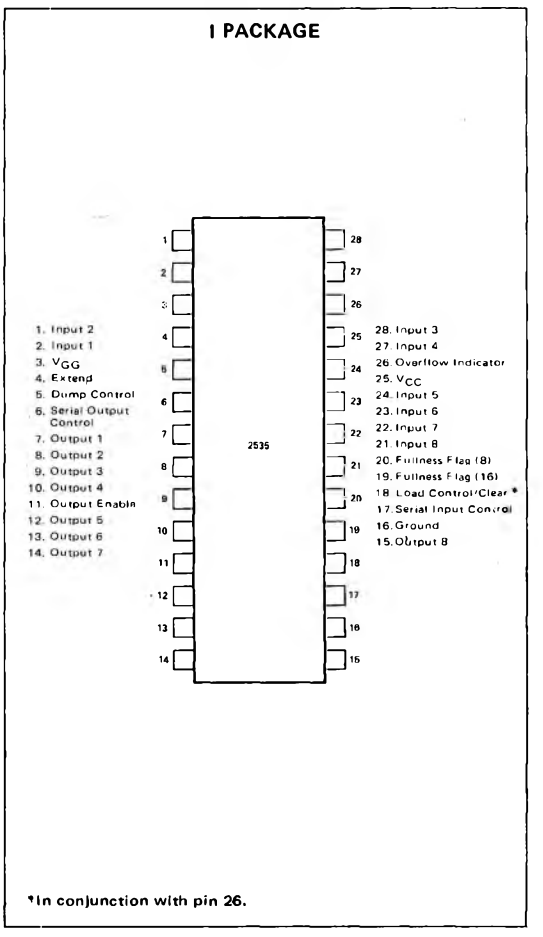
INTERFACE BETWEEN INDEPENDENTLY CLOCKED SYSTEMS
KEYBOARD TO LINE BUFFER MEMORY
DISC AND TAPE BUFFER MEMORIES
DATA CONCENTRATORS
DATA "SILO'S"
BIT RATE SMOOTHING
MODEMS
CPU/TERMINAL BUFFERING

## BIPOLAR COMPATIBILITY

All inputs of the 2535 can be driven directly from TTL output levels. Outputs will sink and source sufficient current for one TTL fan-out.

## PIN CONFIGURATION (TOP VIEW)

I PACKAGE




*In conjunction with pin 26.

## PART IDENTIFICATION

| TYPE | PACKAGE | OP. TEMP. RANGE |
|---|---|---|
| 2535I | 28-Pin Ceramic DIP | 0–70°C |

## MAXIMUM GUARANTEED RATINGS(1)

| | |
|---|---|
| Operating Ambient Temperature | 0°C to 70°C |
| Storage Temperature | −65°C to +150°C |
| Package Power Dissipation(2) @ $T_A$ 70°C | 3.13 W |
| Input(3) and Supply Voltages with respect to $V_{CC}$ | +0.3 to −20 V |

## DC CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{CC}$ = 5 V (8), $V_{DD}$ = GND, $V_{GG}$ = −12 V ±5% unless otherwise noted. (Notes 4,5,6,7,8)

| SYMBOL | TEST | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage | | | 500 | na | $V_{in}$ = GND |
| $I_{LO}$ | Output Leakage (Tri-State Outputs) | | | 500 | na | $V_{out}$ = Chip Enable = GND |
| $V_{IH}$ | Input High Level Voltage (all inputs) | $V_{CC}$ −1.5 | | $V_{CC}$ +0.3 | V | |
| $V_{IL}$ | Input Low Level Voltage (all inputs) | | | $V_{CC}$ −3.8 | V | |
| $V_{OH}$ | Output High Voltage (all outputs) | $V_{CC}$ −2.0 | | | V | $I_{OH}$ = 2.6 mA (source) |
| $V_{OL}$ | Output Low Voltage (all outputs) | | | 0.4 | V | $I_{OL}$ = 1.6 mA (sink) |
| $C_{IN}$ | Input Capacitance (any input) | | 5 | 10 | pF | f = 1 MHz, $V_{IH}$ = $V_{CC}$, 25 mVp-p |
| $C_{OUT}$ | Output Capacitance (any output) | | 5 | 10 | pF | f = 1 MHz, $V_{IH}$ = $V_{CC}$, 25 mVp-p |
| $I_{CC}$ | Power Supply Current | | 60 | | mA | Outputs open, Output Enable = 5 V |
| $I_{GG}$ | Power Supply Current | | 10 | | mA | Outputs open, Output Enable = 5 V |

## AC CHARACTERISTICS

$T_A$ = 0°C to 70°C, $V_{CC}$ = 5 V (8), $V_{DD}$ = GND, $V_{GG}$ = −12 V ±5% unless otherwise noted. (Notes 4,5,6,7,8)

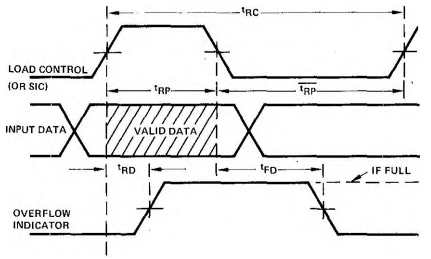
| SYMBOL | TEST | MIN. | TYP. | MAX. | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| $t_{RC}$ | Read-In Cycle Time | 1 | | | μs | |
| $t_{RP}$ | Read-In Pulse Width | 200 | | | ns | |
| $\overline{t_{RP}}$ | Read-In Pulse Width | 400 | | | ns | |
| $t_{RD}$ | Delay from Read-In Rising Edge Time | | | 200 | ns | 1 TTL Load shunted by 20 pF |
| $t_{FD}$ | Delay from Read-In Falling Edge Time | | | 350 | ns | 1 TTL Load shunted by 20 pF |
| $t_{RD}$ | Delay from Read-In Rising Edge Time | | | 120 | ns | MOS Loading Equivalent to 20 pF |
| $t_{FD}$ | Delay from Read-In Falling Edge Time | | | 275 | ns | MOS Loading Equivalent to 20 pF |
| $t_{SR}$ | Shift-Out Cycle Time | 1 | | | μs | |
| $t_{SP}$ | Shift-Out Pulse Width | 200 | | | ns | |
| $t_{SD}$ | Delay from Shift-Out Rising Edge | | | 200 | ns | 1 TTL Load shunted by 20 pF |
| $t_{EX}$ | Extend Time | | | 500 | ns | 1 TTL Load shunted by 20 pF |
| $t_{SD}$ | | | | 130 | ns | MOS Loading Equivalent to 20 pF |
| $t_{EX}$ | | | | 375 | ns | MOS Loading Equivalent to 20 pF |
| $t_{ED}$ | Data Out to Extend Delay | 0 | | | ns | All Data Outputs & Ex with either TTL or MOS loading but not mixed loading |
| $t_{FFD}$ | Fullness-Flag Delay Time | | | 800 | ns | 1 TTL Load shunted by 20 pF |
| $t_{OR}$ | Delay from Output Enable Rising Edge | | | 500 | ns | |
| $t_{OF}$ | Delay from Output Enable Falling Edge | | | 500 | ns | |
| $t_{FT}$ | Fall-Thru Time | | | 2 | μs | 1 TTL Load with 20 pF shunt capacity |

NOTES:

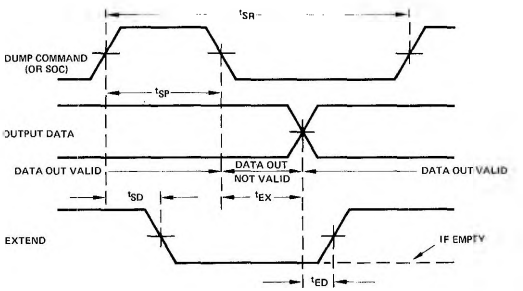
1. Stresses above those listed under "Maximum Guaranteed Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.
2. For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of 48°C/W junction to ambient.
3. All inputs are protected against static charge.
4. Parameters are valid over operating temperature range unless specified.
5. All voltage measurements are referenced to ground.
6. Manufacturer reserves the right to make design and process changes and improvements.
7. Typical values are at +25°C and nominal supply voltages.
8. $V_{CC}$ tolerance is ±5%. Any variation in actual $V_{CC}$ will be tracked directly by $V_{IL}$, $V_{IH}$ and $V_{OH}$ which are stated for a $V_{CC}$ of exactly 5 volts

## TIMING DIAGRAMS

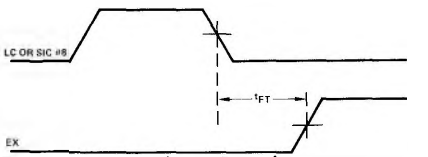
### READ-IN




### SHIFT-OUT

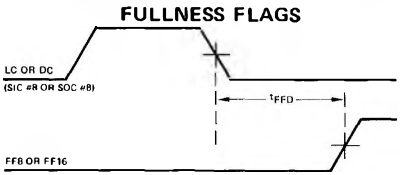



### FALL-THRU TIME

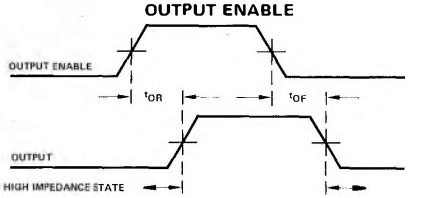



$T_{FT}$ = time required for 1st Byte of data to appear on on outputs from falling edge of Read-In command.

### FULLNESS FLAGS




### OUTPUT ENABLE




## CIRCUIT DESCRIPTION

### INTERNAL ORGANIZATION

The Block Diagram in Figure 1 shows how the data is moved and controlled within the FIFO. The input register accepts either parallel or serial data. Input data is written into the storage array in a location specified by the Write Address Counter. At the same time, the Available Storage Counter is incremented to indicate the fullness condition of the FIFO.

The current output byte is automatically available at the output register. Data may be extracted from the register in parallel or serial form. After the current byte of data is used, the next output byte is read from the storage array at the location specified by the Read Address Counter. At the same time, the Available Storage Counter is decremented to maintain the proper fullness indication.

Two bits of the Available Storage Counter are supplied to the user as Fullness Flags. They indicate the buffer capacity status so that the empty or full conditions can be anticipated. FF8 indicates 1/4 full status, FF16 indicates 1/2 full status and when both flags are up the buffer is 3/4 full.

### INPUT CONTROL

When parallel data is presented to the eight input lines, the Load Command (LC) is pulsed positive to enter the data into the buffer. The input data should remain valid for the width of the LC, and the LC should occur only when the Overflow Indicator (OI) output is low. The OI low signal

## BLOCK DIAGRAM

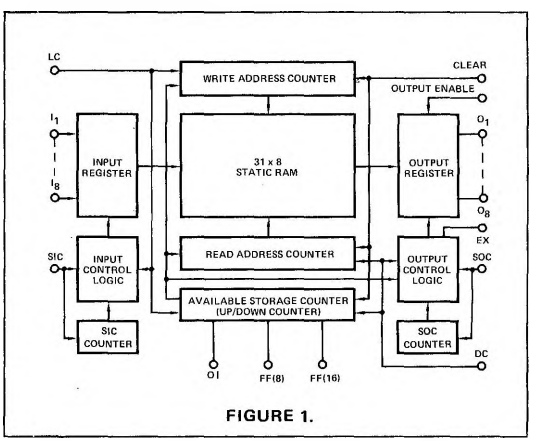



FIGURE 1.

indicates that the input is available for loading. After a delay following the leading edge of the LC, the OI will acknowledge the input by going high. If the OI remains high, then the buffer is full and no new data should be entered. When the OI goes low, the buffer is again available for loading.

Serial data is entered into the input register on Input 1. The Serial Input Clock (SIC) is used to shift the data into the register. OI acknowledges each SIC and the 8th SIC causes the byte in the input register to be inserted into the storage

If LC is pulsed during a serial entry before the 8th SIC, the byte actually entered into the buffer will be a logical OR of the partially entered serial data and the data at the parallel inputs. Bit positions in the input register that have not been shifted into will contain logical zeros.

## OUTPUT CONTROL

When a byte is available in the buffer, it falls through to the output register and is available on the output pins (assuming the Output Enable signal is on). The Extend (EX) signal goes high to indicate that data is available at the output. When the using system is ready for the next byte, it should pulse the Dump Command (DC) line. EX will then go low until the next byte is available. EX stays low if the FIFO is empty.

Serial data is shifted from the output register on Output 8. The Serial Output Clock (SOC) is used to shift the data out of the register and EX responds to each clock pulse. The 8th SOC causes the output control logic to retrieve the next output byte and insert it into the output register.

If DC is pulsed during serial extraction before the 8th SOC, the next output byte is inserted into the output register and the remaining partially shifted data is lost. As the output register is shifted, it is filled with logical zeros.

## BUFFER STORAGE

The first byte inserted into an empty buffer falls all the way through directly to the 8-bit output register. Succeeding input bytes are written into a random access memory array with a capacity of 31 x 8. The array is designed so that it may be addressed at different locations simultaneously. In that way, data may be inserted and removed at the same time. The Write Address Counter controls the locations for storing input data and the Read Address Counter controls the locations from which data is extracted for the output. Both counters are implemented as 31-bit shift registers that move a single bit along their length to directly select the desired word lines in the storage array. This control approach eliminates binary decoding networks and is possible because both the read and write locations are always sequentially accessed.

The use of random access memory to implement the required storage means that the stored data need not be moved around internally. Only the counters that point to the data are manipulated in response to loading and dumping the FIFO. It also means that the fall-through time is minimized since new data in an empty buffer does not have to be shifted sequentially through the buffer before it is available.

## RESET

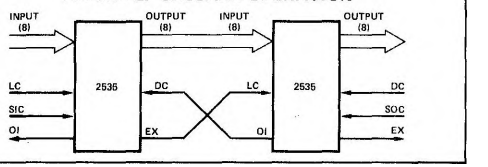
To clear the buffer to its empty state and thus reset all the control counters, two control signals are used. The OI signal, which is normally an output from the FIFO, should be held in a low state by the external reset logic. LC is then pulsed positive for at least 2 microseconds and returned low. The hold on OI is then released, concluding the reset operation.

## EXPANSION

Increased FIFO capacity can be obtained by using multiple 2535's in serial/parallel organizations. Sixteen-bit words, for example, may be buffered by operating two eight bit streams in parallel. In applications where the timing is not critically fast, the LC, SIC, DC, and SOC may be tied together and operated in parallel, but only one each of the OI, EX, and FF signals should be used to control the data flow.

Cascaded operation of more than one FIFO allows expansion to any word depth that is a multiple of 32. The 2535 control signals may be inter-connected without intervening logic to form a FIFO of the desired depth. See Figure 2. Data will automatically fall through to the end of the chain.

FIGURE 2. CASCADE OPERATION




To control two cascaded devices using parallel data interconnection between them, it is only necessary to connect EX from the first device to LC of the second, and OI from the second device to DC of the first. The inputs to the first device and the outputs from the second device may then be operated in the normal modes. When data is entered into the two device combination it falls through to the output of the first device and causes the first EX to go high. The second device sees the EX as a LC, accepts the data, and responds with an OI signal which the first device sees as a DC. In this way the combination acts like one device with twice the capacity and twice the fall-through time of a single 2535.

## FIFO USAGE

Asynchronous FIFO data stream buffering can come in handy in many situations. When a data sink, for example, requires data at a constant rate, the FIFO can provide the constant data stream while at the same time it can absorb data at highly variable rates from the data source.

The reverse situation can also apply. Consider a CRT terminal connected to a computer via a high speed data line. The terminal uses a large recirculating serial memory for data storage. A FIFO in the terminal can accept the constant speed data from the communication line, while at the same time it can wait for synchronization with the circulating memory and then dump a burst of data at high speed.

The circuitry required to implement a FIFO function using SSI and MSI logic can be considerable indeed. In addition to the cost of the logic replaced, the economic evaluation of the FIFO should consider inventory, ordering, testing, reliability, board space, production, design, and debugging problems associated with the old approach. In all of these areas the 2535 can provide significant advantages.