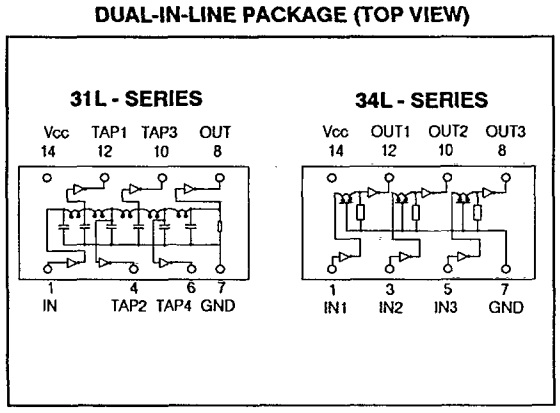
LOW-POWER DELAYS 31L, 34L Series
5 Tap and Triple Independent 14 Pin Moulded DIP

- ❒ Advanced Low-Power Schottky TTL buffered
- ❒ 14 pin package
- ❒ Low profile
- ❒ TTL compatible
- ❒ Industry standard pin-outs

DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The 31L and 34L series of Digital Delay Modules are Advanced Low-Power Schottky TTL buffered delay lines providing precise delay times and direct compatibility with TTL. Five equally spaced delay taps, and triple independent equal delays are each packaged in low profile 14 pin dual-in-line configurations having industry standard pin-outs. Internal termination of the delay line and compensation for propagation delays are incorporated in the design so that no additional external components are required. These modules are particularly suitable for high density board designs.

absolute maximum ratings over operating free-air temperature range

Supply voltage V_{CC} 7V
Input voltage 7V
Min. pulse width as % of total delay 80%
Input pulse repetition rate PRR . . . . . 3 x pulse width min.
Operating free-air temperature range . . . . . 0C to 70C
Storage temperature range . . . . . –55C to 125C
Temperature coefficient of delay . . . . . ±300ppm/C
Lead temperature 1.5mm from case for 10 seconds 300C

drive capabilities

Logic 0 output . . . . . 20 LSTTL loads per tap max.
20 LSTTL loads per unit max.
Logic 1 output . . . . . 20 LSTTL loads per unit max.

electrical specifications over operating free-air temperature range

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH} High-level input voltage		2			V
V_{IL} Low-level input voltage		0.8			V
V_{OH} High-level output voltage	V_{IH} =2V, I_{OH} =−0.4mA Vcc =4.5V to 5.5V	V_{cc}–2			V
V_{OL} Low-level output voltage	Vcc =4.5V I_{OL}=8mA,V_{IL} =0.8V		0.35	0.5	V
I_{IH} High-level input current	Vcc=5.5V, V_{IH}=2.7V			20	μA
I_{IL} Low-level input current	Vcc=5.5V, V_{IL}=0.4V			–0.1	mA
Icc Supply current outputs high	Vcc=5.5V, V_{IL}=0V		0.65	1.1	mA
Icc Supply current outputs low	Vcc=5.5V, V_{IH}=4.5V		2.9	4.2	mA

delay characteristics Vcc = 5V, Ta = 25C, no loads at taps, input test pulse width 100% of total delay, input rise time 3.0ns.

delay tolerance from input to tap ±2ns or ±5% whichever is greater

31L SERIES 5 Tap 14 Pin DIP
Package style H with pins 2, 3, 5, 9, 11 and 13 missing

PART No.	TOTAL DELAY (ns) ±5%	TAP TO TAP DELAY (ns)	OUTPUT RISE TIME (ns)
31L - 5500	50	10 ± 2	8
31L - 5101	100	20 ± 2	8
31L - 5151	150	30 ± 3	8
31L - 5201	200	40 ± 4	8
31L - 5251	250	50 ± 5	8
31L - 5301	300	60 ± 6	8
31L - 5351	350	70 ± 7	8
31L - 5401	400	80 ± 8	8
31L - 5451	450	90 ± 9	8
31L - 5501	500	100 ± 10	8

Note:Delays measured at 1.3V on leading edge, Rise Time measured from 0.8V to 2.0V

31L, 34L Series
5 Tap and Triple Independent 14 Pin Moulded DIP

34L SERIES Triple independent equal 14 Pin DIP
Package style H with pins 2, 4, 6, 9, 11and 13 missing

PART No.	TOTAL DELAY (ns) ±5% (1)	RISE TIME (ns) max.	PART No.	TOTAL DELAY (ns) ±5% (1)	RISE TIME (ns) max.
34L - 010	10	8	34L - 060	60	8
34L - 020	20	8	34L - 070	70	8
34L - 030	30	8	34L - 080	80	8
34L - 040	40	8	34L - 090	90	8
34L - 050	50	8	34L - 100	100	8

Note: Delays measured at 1.3V on leading edge, Rise Time measured from 0.8V to 2.0V
(1) or ±2ns whichever is greater