National Semiconductor

PRELIMINARY

74LCX646
Low-Voltage Octal Transceiver/Register with 5V Tolerant Inputs and Outputs

General Description

The LCX646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops, and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate pin (CPAB or CPBA). The four fundamental handling functions available are illustrated in *Figure 1* through *Figure 4*.

The LCX646 is designed for low voltage (3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

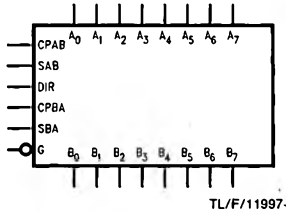
The LCX646 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- Ideal for low power/low noise 2.7V to 3.6V applications
- Power-down static overvoltage protection on inputs and outputs
- Outputs source/sink 24 mA
- Guaranteed simultaneous switching noise level
- Available in SOIC JEDEC and TSSOP
- Implements patented Quiet Series noise/EMI reduction circuitry
- Functionally compatible with the 74 series 646
- Latch performance exceeds 300 mA
- ESD performance:
  Human body Model > 2000V
  Machine Model > 250V

Ordering Code: See Section 11

Logic Symbols



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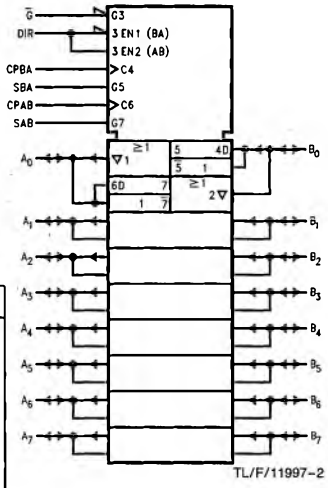
IEEE/IEC



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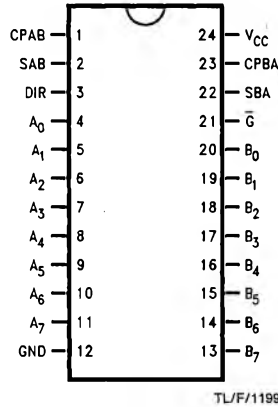
Connection Diagram

Pin Assignment for SOIC and TSSOP



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Pin Names	Description
A_0–A_7	Data Register A Inputs Data Register A Outputs
B_0–B_7	Data Register B Inputs Data Register B Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
$\overline{G}$	Output Enable Input
DIR	Direction Control Input

	SOIC JEDEC	TSSOP JEDEC
Order Number	74LCX646WM 74LCX646WMX	74LCX646MTCX
See NS Package Number	M24B	MTC24

Preliminary Data: National Semiconductor reserves the right to make changes at any time without notice.

Real Time Transfer A-Bus to B-Bus

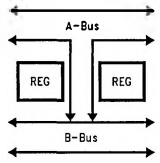

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FIGURE 1

Real Time Transfer B-Bus to A-Bus

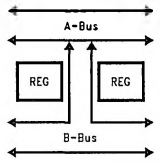

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FIGURE 2

Storage from Bus to Register

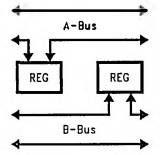

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FIGURE 3

Transfer from Register to Bus

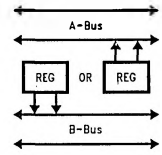

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FIGURE 4

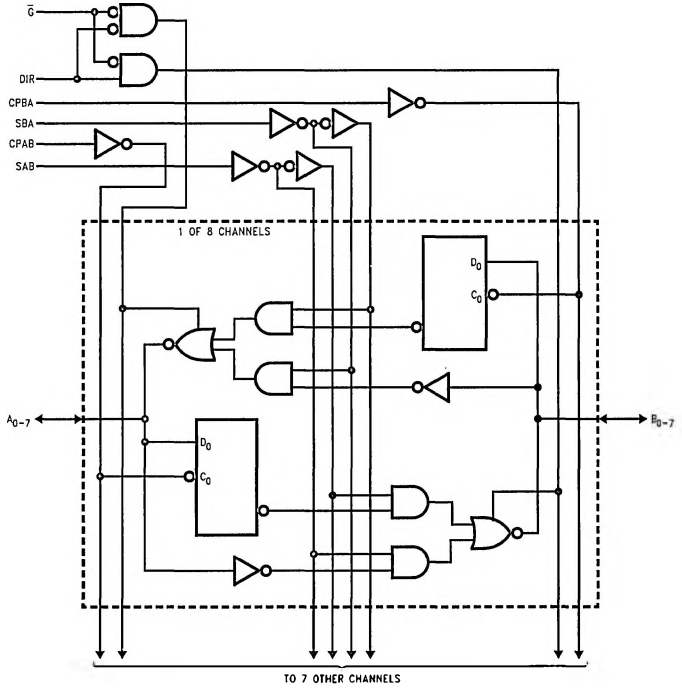
Function Table (Note)

Inputs						Data I/O		Function
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0–A_7	B_0–B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	↑	X	X	X			Clock A_n Data into A Register
H	X	X	↑	X	X			Clock B_n Data into B Register
L	H	X	X	L	X	Input	Output	A_n to B_n—Real Time (Transparent Mode)
L	H	↑	X	L	X			Clock A_n Data into A Register
L	H	H or L	X	H	X			A Register to B_n (Stored Mode)
L	H	↑	X	H	X			Clock A_n Data into A Register and Output to B_n
L	L	X	X	X	L	Output	Input	B_n to A_n—Real Time (Transparent Mode)
L	L	X	↑	X	L			Clock B_n Data into B Register
L	L	X	H or L	X	H			B Register to A_n (Stored Mode)
L	L	X	↑	X	H			Clock B_n Data into B Register and Output to A_n

Note: The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level X = Immaterial L = LOW Voltage Level ↑ = LOW-to-HIGH Transition

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_I)	−0.5V to +7.0V
Output Voltage (V_O)	
Outputs TRI-STATE®	−0.5V to +7.0V
Outputs Active (Note 2)	−0.5V to V_{CC} +0.5V
DC Input Diode Current (I_{IK}) V_I < 0	−50 mA
DC Output Diode Current (I_{OK})	
V_O < 0	−50 mA
V_O > V_{CC}	+50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or Ground Current per Supply Pin (I_{CC} or I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C

Note 1: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Note 2: *I_O Absolute Maximum Rating must be observed.*

Recommended Operating Conditions

Supply Voltage	
Operating	2.0V to 3.6V
Data Retention Only	1.5V to 3.6V
Input Voltage (V_I)	0V to 5.5V
Output Voltage (V_O)	
Output in Active State	0V to V_{CC}
Output In "OFF" State	0V to 5.5V
Output Current I_{OH}/I_{OL}	
V_{CC} = 3.0V to 3.6V	±24 mA
V_{CC} = 2.7V to 3.0V	±12 mA
Free Air Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Ratge ($\Delta t/\Delta V$)	
V_{IN} = 0.8V to 2.0V, V_{CC} = 3.0V	10 ns/V

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40°C to +85°C		Units	Conditions
			Min	Max		
V_{IH}	High Level Input Voltage	2.7–3.6	2.0		V	V_{OUT} ≤ 0.1V or ≥ V_{CC} − 0.1V
V_{IL}	Low Level Input Voltage	2.7–3.6		0.8	V	V_{OUT} ≤ 0.1V or ≥ V_{CC} − 0.1V
V_{OH}	High Level Output Voltage	2.7–3.6	V_{CC} − 0.2		V	I_{OH} = −100 μA
		2.7	2.2		V	I_{OH} = −12 mA
		3.0	2.4		V	I_{OH} = −18 mA
		3.0	2.2		V	I_{OH} = −24 mA
V_{OL}	Low Level Output Voltage	2.7–3.6		0.2	V	I_{OL} = 100 μA
		2.7		0.4	V	I_{OL} = 12 mA
		3.0		0.55	V	I_{OL} = 24 mA
I_I	Input Leakage Current	2.7–3.6		±5.0	μA	0 ≤ V_I ≤ 5.5V
I_{OZ}	TRI-STATE I/O Leakage	2.7–3.6		±5.0	μA	0 ≤ V_O ≤ 5.5V (V_I = V_{IH} or V_{IL})
I_{OFF}	Power Off Leakage Current	0		100	μA	V_I or V_O = 5.5V
I_{CC}	Quiescent Supply Current	2.7–3.6		10	μA	V_I = V_{CC} or GND
				±10	μA	3.6 ≤ (V_I, V_O) ≤ 5.5V
ΔI_{CC}	Increase in I_{CC} per Input	2.7–3.6		500	μA	V_{IH} = V_{CC} − 0.6V

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Max (Note 2)	
t_{PHL}, t_{PLH}	Propagation Delay Bus to Bus	2.7 3.0–3.6	1.5 1.5	8.0 7.0	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Bus	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PHL}, t_{PLH}	Propagation Delay SAB or SBA to A_n or B_n	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PZH}, t_{PZL}	Output Enable Time $\overline{G}$ to A_n or B_n	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time $\overline{G}$ to A_n or B_n	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time DIR to A_n or B_n	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_{PHZ}, t_{PLZ}	Output Disable Time DIR to A_n or B_n	2.7 3.0–3.6	1.5 1.5	9.5 8.5	ns
t_S	Setup Time	2.7 3.0–3.6	2.5 2.5		ns
t_H	Hold Time	2.7 3.0–3.6	1.5 1.5		ns
t_W	Pulde Width	2.7 3.0–3.6	4.0 4.0		ns
t_{OSHL}, t_{OSLH}	Output to Output Skew (Note 1)	3.0		1.0	ns

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design.

Note 2: The maximum AC limits are design targets. Actual performance will be specified upon completion of characterization.

Dynamic Switching Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$ Typical	Units	Conditions
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	3.3	0.8	V	$C_L = 50$ pF, $V_{IH} = 3.3$V, $V_{IL} = 0$V

Capacitance

Symbol	Parameter	Typical	Units	Conditions
C_{IN}	Input Capacitance	7	pF	V_{CC} = Open $V_I = 0$V or V_{CC}
$C_{I/O}$	Input/Output Capacitance	8	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC}
C_{PD}	Power Dissipation Capacitance	32	pF	$V_{CC} = 3.3$V $V_I = 0$V or V_{CC} F = 10 MHz