

74LVX02

Low Voltage Quad 2-Input NOR Gate

General Description

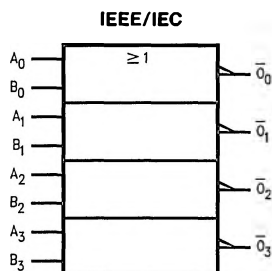
The LVX02 contains four 2-input NOR gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

Features

- ▣ Input voltage level translation from 5V to 3V
- ▣ Ideal for low power/low noise 3.3V applications
- ▣ Available in SOIC JEDEC, SOIC EIAJ and SSOP packages
- ▣ Guaranteed simultaneous switching noise level and dynamic threshold performance

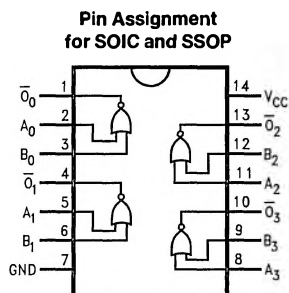
Ordering Code: See Section 11

Logic Symbol



TL/F/11600-2

Connection Diagram



TL/F/11600-1

Pin Names	Description
A_n, B_n	Inputs
$\bar{O}_n$	Outputs

	SOIC JEDEC	SOIC EIAJ	SSOP TYPE I
Order Number	74LVX02M 74LVX02MX	74LVX02SJ 74LVX02SJX	74LVX02MSCX
See NS Package Number	M14A	M14D	MSC14

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}) $-0.5V$ to $+7.0V$

DC Input Diode Current (I_{IK})
 $V_I = -0.5V$ -20 mA

DC Input Voltage (V_I) $-0.5V$ to $7V$

DC Output Diode Current (I_{OK})
 $V_O = -0.5V$ -20 mA
 $V_O = V_{CC} + 0.5V$ $+20$ mA

DC Output Voltage (V_O) $-0.5V$ to $V_{CC} + 0.5V$

DC Output Source
or Sink Current (I_O) ± 25 mA

DC V_{CC} or Ground Current
(I_{CC} or I_{GND}) ± 50 mA

Storage Temperature (T_{STG}) $-65^\circ C$ to $+150^\circ C$

Power Dissipation 180 mW

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Supply Voltage (V_{CC}) $2.0V$ to $3.6V$

Input Voltage (V_I) $0V$ to $5.5V$

Output Voltage (V_O) $0V$ to V_{CC}

Operating Temperature (T_A) $-40^\circ C$ to $+85^\circ C$

Input Rise and Fall Time ($\Delta t/\Delta v$) 0 ns/V to 100 ns/V

DC Electrical Characteristics

Symbol	Parameter	V _{CC}	74LVX02			74LVX02		Units	Conditions	
			T _A = +25°C			T _A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V _{IH}	High Level Input Voltage	2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V		
V _{IL}	Low Level Input Voltage	2.0 3.0 3.6	0.5 0.8 0.8			0.5 0.8 0.8		V		
V _{OH}	High Level Output Voltage	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V	V _{IN} = V _{IL} or V _{IH}	I _{OH} = −50 μA I _{OH} = −50 μA I _{OH} = −4 mA
V _{OL}	Low Level Output Voltage	2.0 3.0 3.0		0.0 0.0 0.36	0.1 0.1	0.1 0.1 0.44		V	V _{IN} = V _{IL} or V _{IH}	I _{OL} = 50 μA I _{OL} = 50 μA I _{OL} = 4 mA
I _{IN}	Input Leakage Current	3.6	±0.1			±1.0		μA	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	3.6	2.0			20.0		μA	V _{IN} = V _{CC} or GND	

Noise Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	74LVX02		Units	Conditions C _L (pF)
			T _A = 25°C			
			Typ	Limit		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3	0.3	0.5	V	50
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3	−0.3	−0.5	V	50
V _{IHD}	Minimum High Level Dynamic Input Voltage	3.3		2.0	V	50
V _{ILD}	Maximum Low Level Dynamic Input Voltage	3.3		0.8	V	50

Note: (Input t_r = t_f = 3 ns)

AC Electrical Characteristics: See Section 2 for Test Methodology

Symbol	Parameter	V _{CC} (V)	74LVX02			74LVX02		Units	C _L (pF)
			T _A = +25°C			T _A = −40°C to +85°C			
			Min	Typ	Max	Min	Max		
t _{PLH} , t _{PHL}	Propagation Delay Time	2.7	5.9	10.7	1.0	13.5	ns	15	
			8.4	14.2	1.0	17.0		50	
		3.3 ± 0.3	4.5	6.6	1.0	8.0		15	
			7.0	10.1	1.0	11.5		50	
t _{OSLH} , t _{OSHL}	Output to Output Skew (Note 1)	2.7	1.5			1.5	ns	50	

Note 1: Parameter guaranteed by design. t_{OSLH} = |t_{PLHm} - t_{PLHl}|, t_{OSHL} = |t_{PHLm} - t_{PHLl}|

Capacitance

Symbol	Parameter	74LVX02			74LVX02		Units
		T _A = +25°C			T _A = −40°C to +85°C		
		Min	Typ	Max	Min	Max	
C _{IN}	Input Capacitance		4	10		10	pF
C _{PD}	Power Dissipation Capacitance (Note 1)		15				pF

Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation: $I_{CC(opr)} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{4 \text{ (per Gate)}}$