

SCHOTTKY BIPOLAR 8205

APPLICATIONS OF THE 8205

The 8205 can be used in a wide variety of applications in microcomputer systems. I/O ports can be decoded from the address bus, chip select signals can be generated to select memory devices and the type of machine state such as in 8008 systems can be derived from a simple decoding of the state lines (S0, S1, S2) of the 8008 CPU.

I/O Port Decoder

Shown in the figure below is a typical application of the 8205. Address input lines are decoded by a group of 8205s (3). Each input has a binary weight. For example, A0 is assigned a value of 1 and is the LSB; A4 is assigned a value of 16 and is the MSB. By connecting them to the decoders as shown, an active low signal that is exclusive in nature and represents the value of the input address lines, is available at the outputs of the 8205s.

This circuit can be used to generate enable signals for I/O ports or any other decoder related application.

Note that no external gating is required to decode up to 24 exclusive devices and that a simple addition of an inverter or two will allow expansion to even larger decoder networks.

Chip Select Decoder

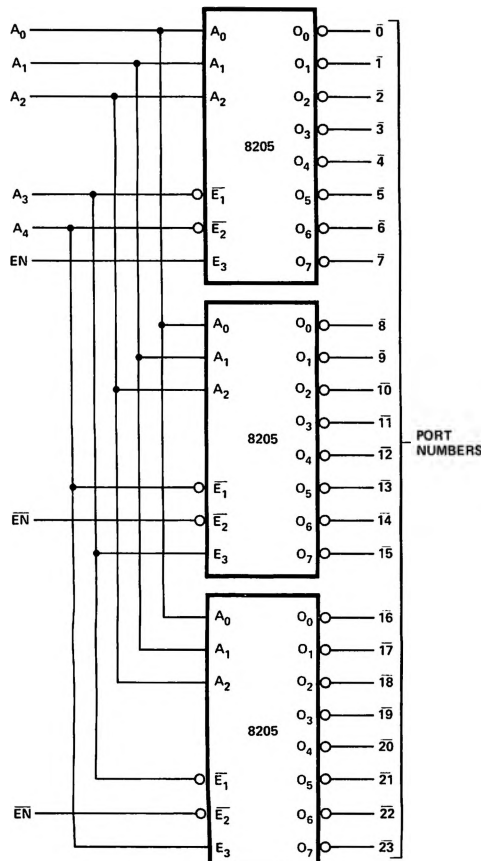
Using a very similar circuit to the I/O port decoder, an ar-

ray of 8205s can be used to create a simple interface to a 24K memory system.

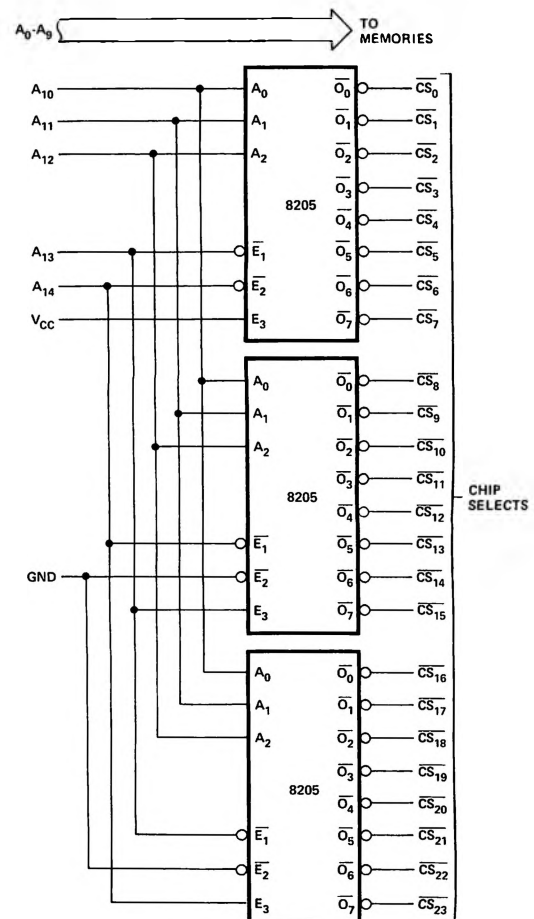
The memory devices used can be either ROM or RAM and are 1K in storage capacity. 8308s and 8102s are the devices typically used for this application. This type of memory device has ten (10) address inputs and an active "low" chip select (\overline{CS}). The lower order address bits A0-A9 which come from the microprocessor are "bussed" to all memory elements and the chip select to enable a specific device or group of devices comes from the array of 8205s. The output of the 8205 is active low so it is directly compatible with the memory components.

Basic operation is that the CPU issues an address to identify a specific memory location in which it wishes to "write" or "read" data. The most significant address bits A10-A14 are decoded by the array of 8205s and an exclusive, active low, chip select is generated that enables a specific memory device. The least significant address bits A0-A9 identify a specific location within the selected device. Thus, all addresses throughout the entire memory array are exclusive in nature and are non-redundant.

This technique can be expanded almost indefinitely to support even larger systems with the addition of a few inverters and an extra decoder (8205).



I/O Port Decoder



24K Memory Interface

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Logic Element Example

Probably the most overlooked application of the 8205 is that of a general purpose logic element. Using the "on-chip" enabling gate, the 8205 can be configured to gate its decoded outputs with system timing signals and generate strobes that can be directly connected to latches, flip-flops and one-shots that are used throughout the system.

An excellent example of such an application is the "state decoder" in an 8008 CPU based system. The 8008 CPU issues three bits of information (S₀, S₁, S₂) that indicate the nature of the data on the Data Bus during each machine state. Decoding of these signals is vital to generate strobes that can load the address latches, control bus discipline and general machine functions.

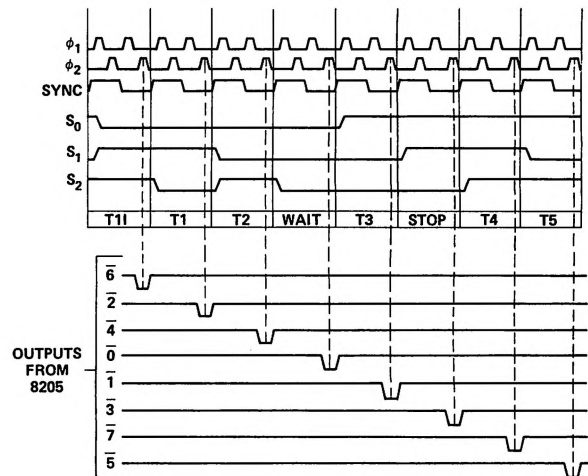
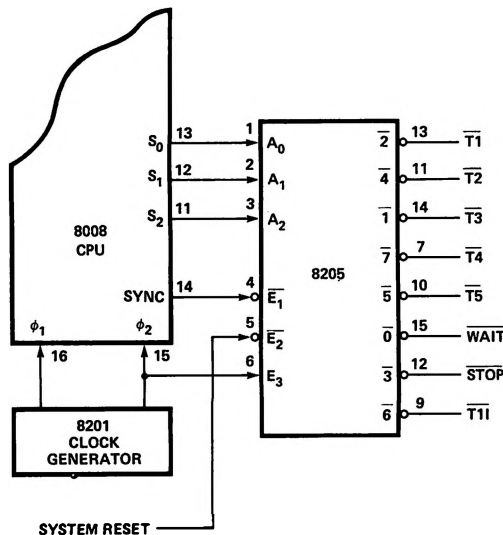
In the figure below a circuit is shown using the 8205 as the "state decoder" for an 8008 CPU that not only decodes the S₀, S₁, S₂ outputs but gates these signals with the clock (phase 2) and the SYNC output of the 8008 CPU. The $\overline{T1}$

and $\overline{T2}$ decoded strobes can connect directly to devices like 8212s for latching the address information. The other decoded strobes can be used to generate signals to control the system data bus, memory timing functions and interrupt structure. RESET is connected to the enable gate so that strobes are not generated during system reset, eliminating accidental loading.

The power of such a circuit becomes evident when a single decoded strobe is logically broken down. Consider $\overline{T1}$ output, the boolean equation for it would be:

$$\overline{T1} = (\overline{S0} \cdot S1 \cdot \overline{S2}) \cdot (\overline{SYNC} \cdot \text{Phase 2} \cdot \overline{\text{Reset}})$$

A six input NAND gate plus a few inverters would be needed to implement this function. The seven remaining outputs would need a similar circuit to duplicate their function, obviously a substantial savings in components can be achieved when using such a technique.



State Control Coding

S ₀	S ₁	S ₂	STATE
0	1	0	T1
0	1	1	T11
0	0	1	T2
0	0	0	WAIT
1	0	0	T3
1	1	0	STOP
1	1	1	T4
1	0	1	T5

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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias:	Ceramic	-65°C to +125°C
	Plastic	-65°C to +75°C
Storage Temperature		-65°C to +160°C
All Output or Supply Voltages		-0.5 to +7 Volts
All Input Voltages		-1.0 to +5.5 Volts
Output Currents		125 mA

*COMMENT

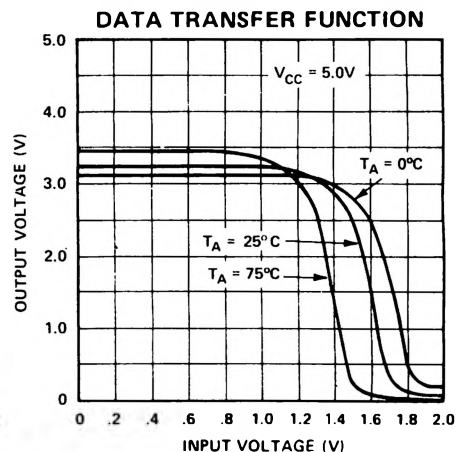
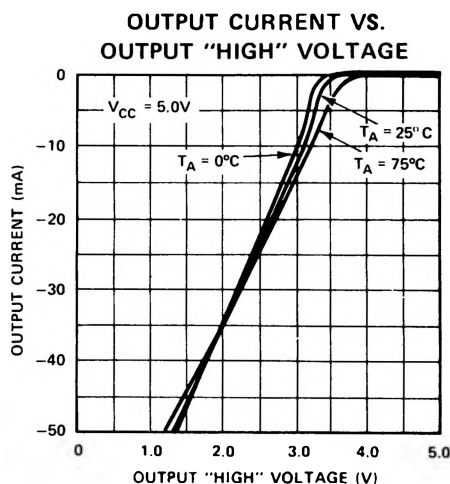
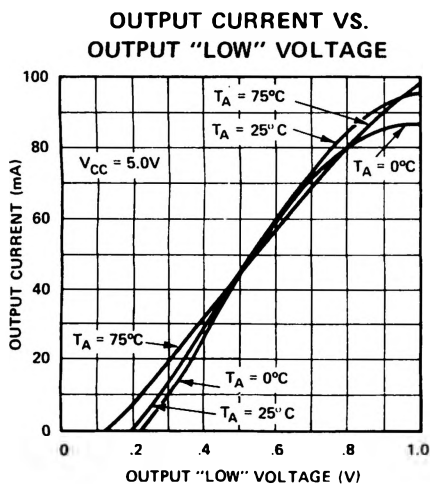
Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

8205

SYMBOL	PARAMETER	LIMIT		UNIT	TEST CONDITIONS
		MIN.	MAX.		
I_F	INPUT LOAD CURRENT		-0.25	mA	$V_{CC} = 5.25\text{V}$, $V_F = 0.45\text{V}$
I_R	INPUT LEAKAGE CURRENT		10	μA	$V_{CC} = 5.25\text{V}$, $V_R = 5.25\text{V}$
V_C	INPUT FORWARD CLAMP VOLTAGE		-1.0	V	$V_{CC} = 4.75\text{V}$, $I_C = -5.0\text{ mA}$
V_{OL}	OUTPUT "LOW" VOLTAGE		0.45	V	$V_{CC} = 4.75\text{V}$, $I_{OL} = 10.0\text{ mA}$
V_{OH}	OUTPUT HIGH VOLTAGE	2.4		V	$V_{CC} = 4.75\text{V}$, $I_{OH} = -1.5\text{ mA}$
V_{IL}	INPUT "LOW" VOLTAGE		0.85	V	$V_{CC} = 5.0\text{V}$
V_{IH}	INPUT "HIGH" VOLTAGE	2.0		V	$V_{CC} = 5.0\text{V}$
I_{SC}	OUTPUT HIGH SHORT CIRCUIT CURRENT	-40	-120	mA	$V_{CC} = 5.0\text{V}$, $V_{OUT} = 0\text{V}$
V_{OX}	OUTPUT "LOW" VOLTAGE @ HIGH CURRENT		0.8	V	$V_{CC} = 5.0\text{V}$, $I_{OX} = 40\text{ mA}$
I_{CC}	POWER SUPPLY CURRENT		70	mA	$V_{CC} = 5.25\text{V}$

TYPICAL CHARACTERISTICS



SCHOTTKY BIPOLAR 8205

8205 SWITCHING CHARACTERISTICS

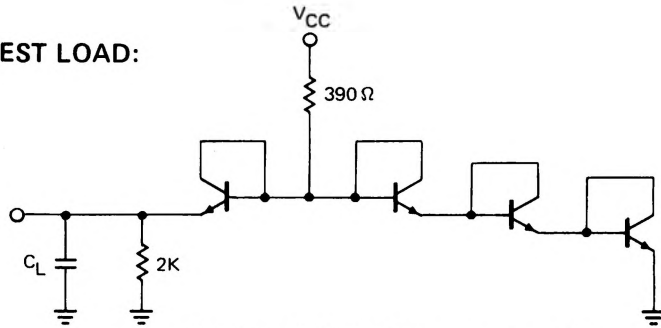
CONDITIONS OF TEST:

Input pulse amplitudes: 2.5V

Input rise and fall times: 5 nsec
between 1V and 2V

Measurements are made at 1.5V

TEST LOAD:

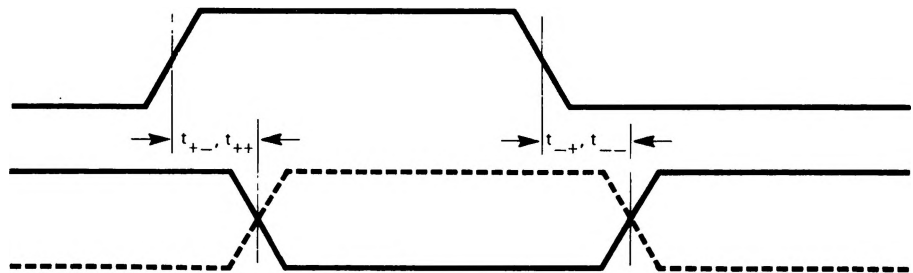


All Transistors 2N2369 or Equivalent. $C_L = 30 \text{ pF}$

TEST WAVEFORMS

ADDRESS OR ENABLE
INPUT PULSE

OUTPUT



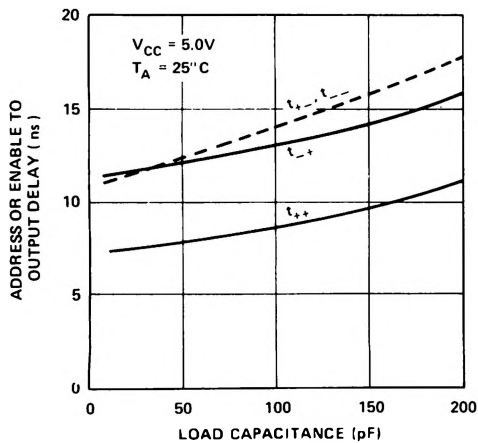
A.C. CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$ unless otherwise specified.

SYMBOL	PARAMETER	MAX. LIMIT	UNIT	TEST CONDITIONS
t_{++}	ADDRESS OR ENABLE TO OUTPUT DELAY	18	ns	
t_{-+}		18	ns	
t_{+-}		18	ns	
t_{--}		18	ns	
$C_{IN}^{(1)}$	INPUT CAPACITANCE	P8205 4(typ.)	pF	$f = 1 \text{ MHz}$, $V_{CC} = 0\text{V}$ $V_{BIAS} = 2.0\text{V}$, $T_A = 25^\circ\text{C}$
		C8205 5(typ.)	pF	

1. This parameter is periodically sampled and is not 100% tested.

TYPICAL CHARACTERISTICS

ADDRESS OR ENABLE TO OUTPUT
DELAY VS. LOAD CAPACITANCE



ADDRESS OR ENABLE TO OUTPUT
DELAY VS. AMBIENT TEMPERATURE

