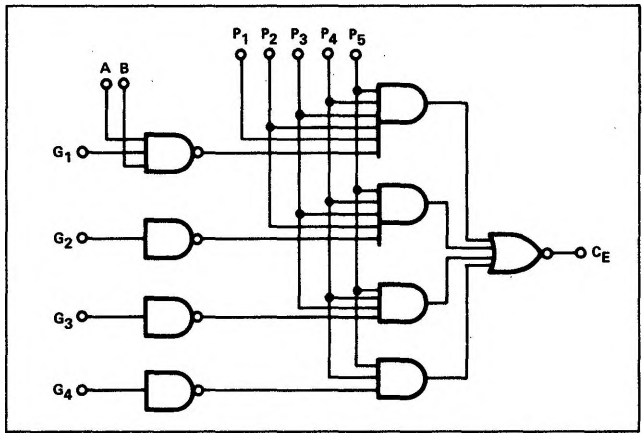
DESCRIPTION

The 8261 Fast Carry Extender is a monolithic gate array designed specifically to be used in conjunction with the 8260 Arithmetic Logic element. A 8260/8261 combination facilitates the implementation of the look-ahead technique in adder systems, thus considerably improving propagation times. The circuit structure of this array is of the familiar TTL type.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS (Over Recommended Operating Temperature And Voltage)

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					DRIVEN INPUTS		OTHER INPUTS			
	MIN.	TYP.	MAX.	UNITS	G,A,B	P	G,A,B	P		
"1" Output Voltage	2.6	3.5		V	2.0V				-800μA	6
"0" Output Voltage			0.4	V	0.8V		4.75V	4.75V	9.6mA	7
"1" Input Current										
G Input			40	μA	4.5V		A = 0V			
A and B Inputs			40	μA	4.5V		G_1 = 0V			
P_1 Input			40	μA		4.5V		0V		
P_2 Input			80	μA		4.5V		0V		
P_3 Input			120	μA		4.5V		0V		
P_4 and P_5 Inputs			160	μA		4.5V		0V		
"0" Input Current										
G, A and B			-1.6	mA	0.4V			5.25V		
P_1 Input			-1.6	mA		0.4V	0V	5.25V		
P_2 Input			-3.2	mA		0.4V	0V	5.25V		
P_3 Input			-4.8	mA		0.4V	0V	5.25V		
P_4 and P_5 Inputs			-6.4	mA		0.4V	0V	5.25V		
Power/Current Consumption		95/18.1	140/26.6	mW/mA			5.25V	0V		12

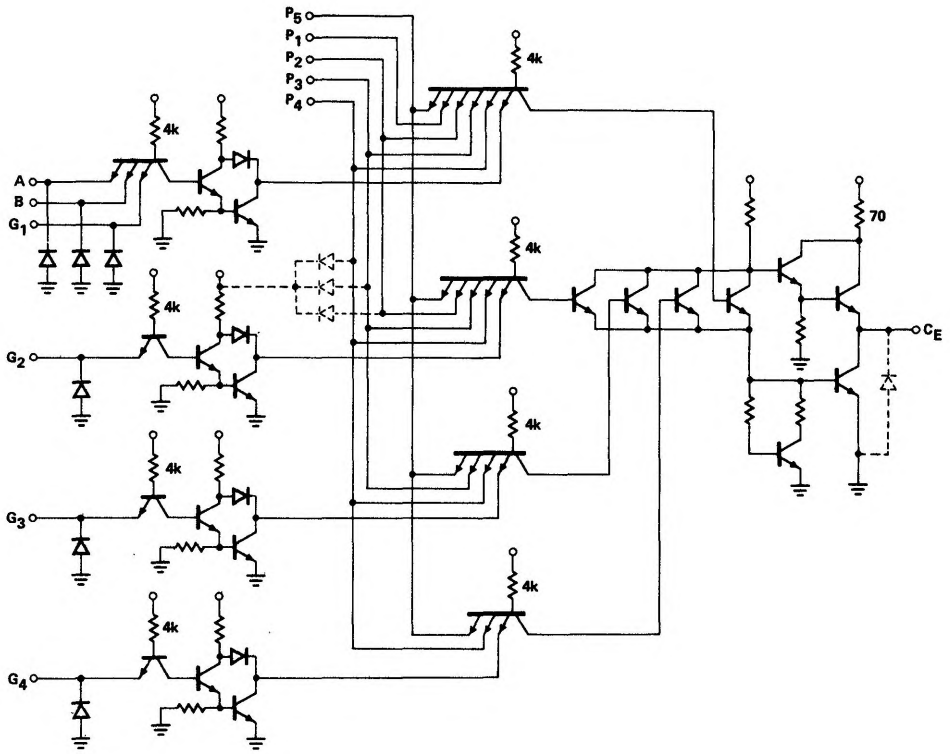
T_A = 25° C and V_{CC} = 5.0V

CHARACTERISTICS	LIMITS				TEST CONDITIONS				OUTPUTS	NOTES
					DRIVEN INPUTS		OTHER INPUTS			
	MIN.	TYP.	MAX.	UNITS	G,A,B	P	G,A,B	P		
Turn-on Delay										
G to C_E		16	25	ns						8
P to C_E		15	25	ns						8
Turn-off Delay										
G to C_E		15	23	ns						8
P to C_E		8	15	ns						8
Input Latch Voltage	5.5			V	10mA	10mA	0V	0V		9
Output Short Circuit Current	-20		-70	mA	5.0V	0V			0V	

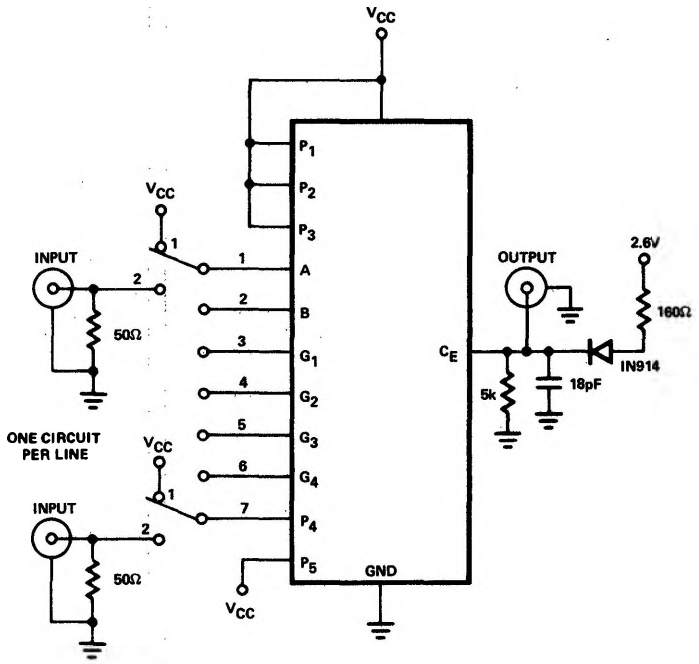
NOTES:

1. All voltage and current measurements are referenced to the ground terminal. Input terminals not specifically referenced are tied to V_{CC}.
2. All measurements are taken with ground pin tied to zero volts.
3. Positive current flow is defined as into the terminal referenced.
4. Positive logic definition:
   "UP" Level = "1", "DOWN" Level = "0".
5. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
6. Output source current is supplied through a resistor to ground.
7. Output sink current is supplied through a resistor to V_{CC}.
8. Refer to AC Test Figure.
9. This test guarantees operation free of input latch-up over the specified operating power supply voltage range.
10. Manufacturer reserves the right to make design and process changes and improvements.
11. Input "0" thresholds for P_1 through P_5 inputs are guaranteed to be 0.7 volts.
12. V_{CC} = 5.25V.

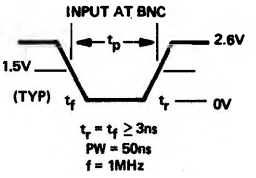
SCHEMATIC DIAGRAM

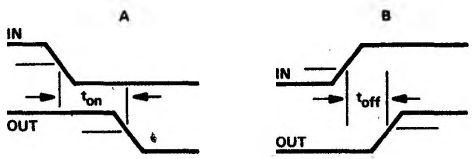


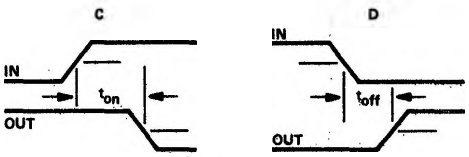
AC TEST FIGURE AND WAVEFORMS



SWITCH NO. / PIN DES.	SWITCH POSITION 1	2	3	4	5	6	7	WAVEFORM TYPE
A	2	1	1	1	1	1	1	
B	1	2	1	1	1	1	1	
G_1	1	1	2	1	1	1	1	
G_2	1	1	1	2	1	1	1	A and B
G_3	1	1	1	1	2	1	1	
G_4	1	1	1	1	1	2	1	
P_4								
STEP A	2	1	1	1	1	1	2	
STEP B	1	2	1	1	1	1	2	
STEP C	1	1	2	1	1	1	2	
STEP D	1	1	1	2	1	1	2	C and D
STEP E	1	1	1	1	2	1	2	
STEP F	1	1	1	1	1	2	2	

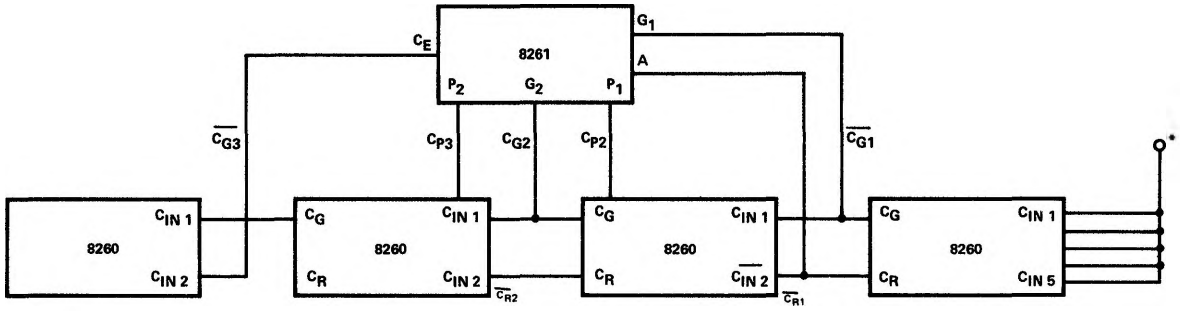






NOTES:
1. Scope terminals to be ≤ 1-1/2" from package pins.
2. Position 1 on all switches provides a logical "1". Position 2 on all switches provides a logical "0" when input signal is not present.
3. All measurements are made at 1.5 volts level.

TYPICAL APPLICATION



16 BIT, T_A = 42ns, typical Fast Adder System (5 packages)
*Tied to V_{CC} if not-true inputs are used, otherwise to ground. Unused 8261 pins should be tied to V_{CC}.