

OBJECTIVE SPECIFICATION

82S400/400A - I • 82S401/401A - I

DESCRIPTION

The 82S400 and 82S401, with typical access time of 45ns, are ideal for cache buffer applications and for systems requiring very high speed main memory. The 82S400A and 82S401A are devices selected for speed compatibility with industry standard 1024-bit RAMs having 45ns access time.

Both devices require a single +5V power supply, feature very low current pnp input structures, and include on-chip decoding and a chip enable input for ease of memory expansion. They feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

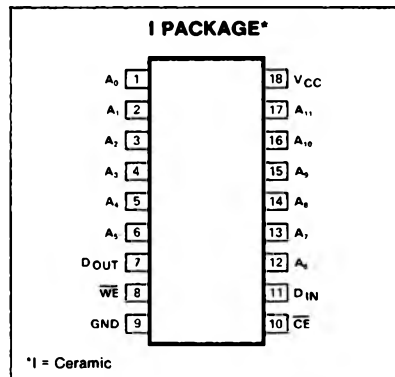
APPLICATIONS

- High speed main frame
- Cache memory
- Buffer storage
- Writable control store

FEATURES

- Address access time:
82S400/401: 70ns max
82S400A/401A: 45ns max
- Write cycle time: 70ns max
- Power dissipation: 0.12mW/bit typ
- Input loading: $-150\mu\text{A}$ max
- On-chip address decoding
- Output options:
82S400: Open collector
82S401: Tri-state
- Non-inverting output
- Blanked output during Write
- Fully TTL compatible

PIN CONFIGURATION

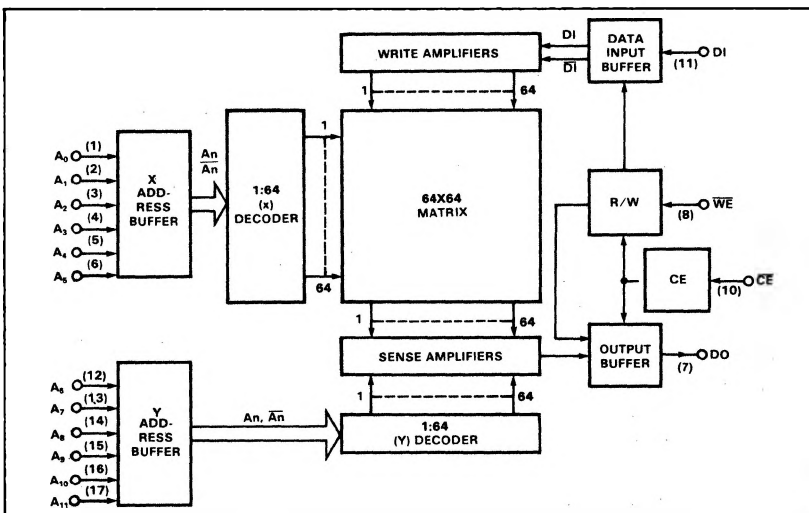


TRUTH TABLE

MODE	$\overline{\text{CE}}$	$\overline{\text{WE}}$	D_{IN}	D_{OUT}	
				82S400	82S401
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER ¹	RATING	UNIT
V _{CC} Power supply voltage	+7	Vdc
V _{IN} Input voltage	+5.5	Vdc
V _{OH} Output voltage	+5.5	Vdc
V _O Off-state (82S401)	+5.5	Vdc
Temperature range		°C
T _A Operating	0 to +75	
T _{STG} Storage	-65 to +150	

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DC ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ ²	Max	
V_{IL} V_{IH} V_{IC}	Input voltage Low ¹ High ¹ Clamp ^{1,3}	$V_{CC} = \text{Min}$ $V_{CC} = \text{Max}$ $V_{CC} = \text{Min}, I_{IN} = -12\text{mA}$	2.0	-1.0	.85 -1.5	V
V_{OL} V_{OH}	Output voltage Low ^{1,4} High (82S401) ^{1,5}	$V_{CC} = \text{Min}$ $I_{OL} = 16\text{mA}$ $I_{OH} = -2\text{mA}$	2.4	0.35	0.45	V
I_{IL} I_{IH}	Input current Low High	$V_{IN} = 0.45\text{V}$ $V_{IN} = 5.5\text{V}$		-25 1	-150 25	μA
I_{OLK} $I_{O(\text{OFF})}$ I_{OS}	Output current Leakage (82S400) ⁶ Hi-Z state (82S401) ⁶ Short circuit (82S401) ⁷	$V_{CC} = \text{Max}$ $V_{OUT} = 5.5\text{V}$ $V_{OUT} = 5.5\text{V}$ $V_{OUT} = 0.45\text{V}$ $V_{OUT} = 0\text{V}$	-20	1 1 -1	40 60 -60 -100	μA μA mA
I_{CC}	V_{CC} supply current ⁸	$V_{CC} = \text{Max}$ $0 < T_A < 25^{\circ}\text{C}$ $T_A \geq 25^{\circ}\text{C}$		120 105	155 130	mA
C_{IN} C_{OUT}	Capacitance Input Output	$V_{CC} = 5.0\text{V}$ $V_{IN} = 2.0\text{V}$ $V_{OUT} = 2.0\text{V}$		4 7		pF

AC ELECTRICAL CHARACTERISTICS $0^{\circ} \leq T_A \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$, $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30\text{pF}$

PARAMETER	TO	FROM	N82S400A/401A			N82S400/401			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
T_{AA} T_{CE}	Access time Output	Address Chip enable			45 30		45 30	70 45	ns
T_{CD} T_{WD}	Disable time Output	Chip enable Write enable			30 30		30 30	45 45	ns
T_{WR}	Recovery time Output	Write enable			30		30	45	ns
T_{WSA} T_{WHA}	Setup and hold time Setup time Hold time	Write enable Address	5			10	5		ns
T_{WSD} T_{WHD}	Setup time Hold time	Write enable Data in	35 5			50 10	35 5		
T_{WSC} T_{WHC}	Setup time Hold time	Write enable CE	5			10	5		
T_{WP}	Pulse width ⁹ Write enable		35			50	35		ns

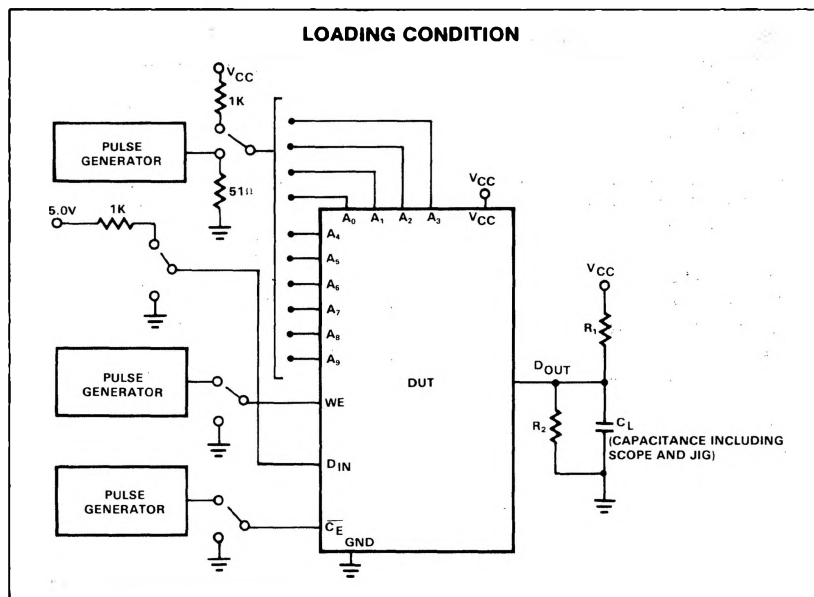
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^{\circ}\text{C}$.
3. Test each input one at a time.
4. Measured with a logic low stored. Output sink current is supplied through a resistor to V_{CC} .
5. Measured with V_{IL} applied to $\overline{\text{CE}}$ and a logic high stored.
6. Measured with V_{IH} applied to $\overline{\text{CE}}$.
7. Duration of the short circuit should not exceed 1 second.
8. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
9. Minimum required to guarantee a Write into the slowest bit.
10. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
 θ_{JA} junction to ambient at 400fpm air flow - $50^{\circ}\text{C}/\text{watt}$
 θ_{JA} junction to ambient - still air - $90^{\circ}\text{C}/\text{watt}$
 θ_{JA} junction to case - $20^{\circ}\text{C}/\text{watt}$

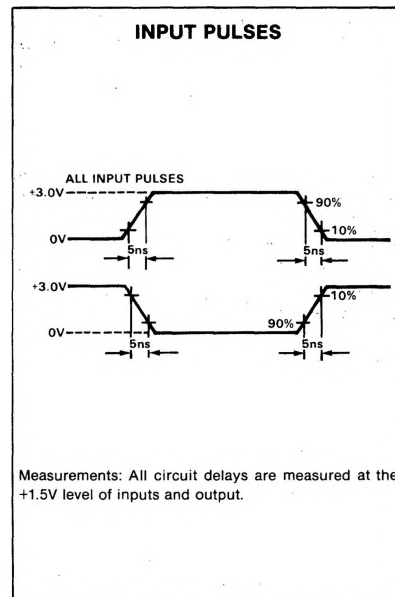
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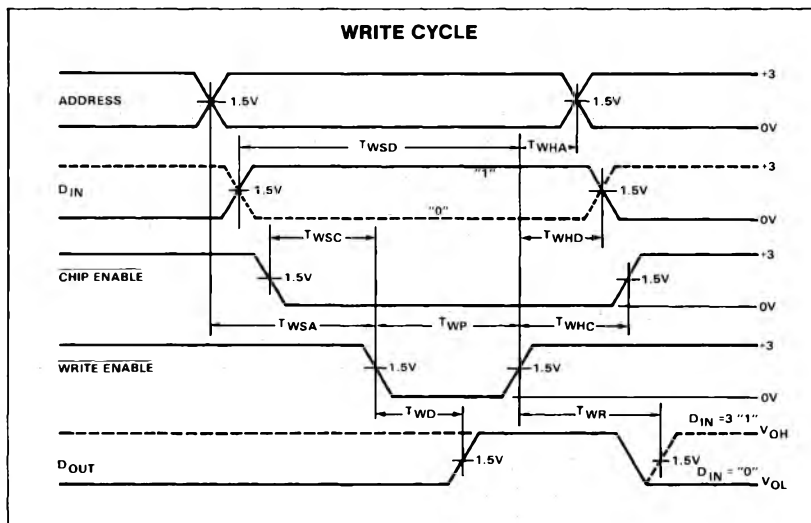
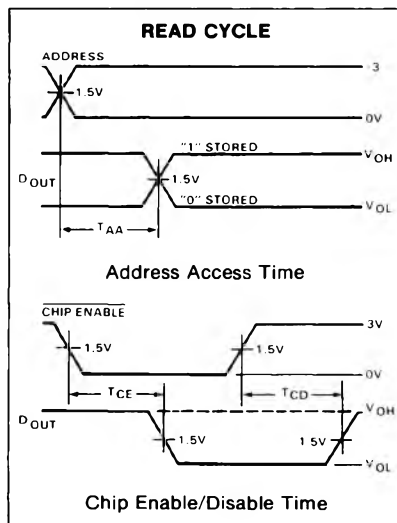
TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



TIMING DIAGRAMS



TIMING DEFINITIONS

T_{WR}	Delay between end of Write Enable pulse and when Data Output becomes valid (assuming Address still valid—not as shown).
T_{CE}	Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes high and Data Output is in off state.
T_{AA}	Delay between beginning of valid

T_{WSD}	Required delay between beginning of valid Data Input and when Data Output becomes valid.
T_{WSC}	Required delay between beginning of valid Chip Enable and beginning of Write Enable pulse.
T_{WHD}	Required delay between end of Write Enable pulse and end of valid Input Data.
T_{WHP}	Width of Write Enable pulse.
T_{WSA}	Required delay between beginning of valid Address and beginning of Write Enable pulse.

T_{WSD}	Required delay between beginning of valid Data Input and end of Write Enable pulse.
T_{WD}	Delay between beginning of Write Enable pulse and when Data Output is in off state.
T_{WHC}	Required delay between end of Write Enable pulse and end of Chip Enable.
T_{WHA}	Required delay between end of Write Enable pulse and end of valid Address.