

# CAT5116

## Log-Taper, 100-Tap Digitally Programmable Potentiometer (DPP)

### Description

The CAT5116 is a log-taper single digitally programmable potentiometer (DPP) designed as an electronic replacement for mechanical potentiometers.

Ideal for automated adjustments on high volume production lines, DPP ICs are well suited for applications where equipment requiring periodic adjustment is either difficult to access or located in a hazardous or remote environment.

The CAT5116 contains a 100-tap series resistor array connected between two terminals  $R_H$  and  $R_L$ . An up/down counter and decoder that are controlled by three input pins, determines which tap is connected to the wiper,  $R_W$ .

The wiper setting, stored in nonvolatile memory, is not lost when the device is powered down and is automatically reinstated when power is returned. The wiper can be adjusted to test new system values without effecting the stored setting.

Wiper-control of the CAT5116 is accomplished with three input control pins,  $\overline{CS}$ ,  $U/\overline{D}$ , and  $\overline{INC}$ . The  $\overline{INC}$  input increments the wiper in the direction which is determined by the logic state of the  $U/\overline{D}$  input. The  $\overline{CS}$  input is used to select the device and also store the wiper position prior to power down.

The digitally programmable potentiometer can be used as a three-terminal resistive divider or as a two-terminal variable resistor.

### Features

- 100-position, Log-taper Potentiometer
- Non-volatile EEPROM Wiper Storage
- 10 nA Ultra-low Standby Current
- Single-supply Operation: 2.5 V – 5.5 V
- Increment Up/Down Serial Interface
- Resistance Value: 32 k $\Omega$
- Available in 8-pin MSOP, TSSOP, SOIC and DIP Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

- Automated Product Calibration
- Remote Control Adjustments
- Offset, Gain and Zero Control
- Audio Volume Control
- Sensor Adjustment
- Motor Controls and Feedback Systems
- Programmable Analog Functions



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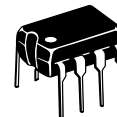
<http://onsemi.com>



SOIC-8  
V SUFFIX  
CASE 751BD



MSOP-8  
Z SUFFIX  
CASE 846AD

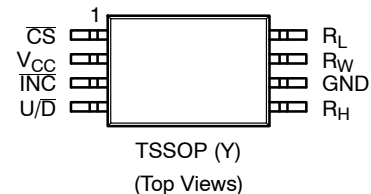
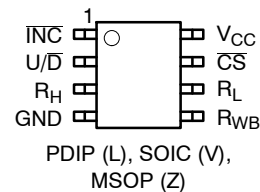


PDIP-8  
L SUFFIX  
CASE 646AA



TSSOP-8  
Y SUFFIX  
CASE 948AL

### PIN CONFIGURATIONS



### PIN FUNCTION

Pin Name	Function
$\overline{INC}$	Increment Control
$U/\overline{D}$	Up/Down Control
$R_H$	Potentiometer High Terminal
GND	Ground
$R_W$	Buffered Wiper Terminal
$R_L$	Potentiometer Low Terminal
$\overline{CS}$	Chip Select
$V_{CC}$	Supply Voltage

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

Functional Diagram

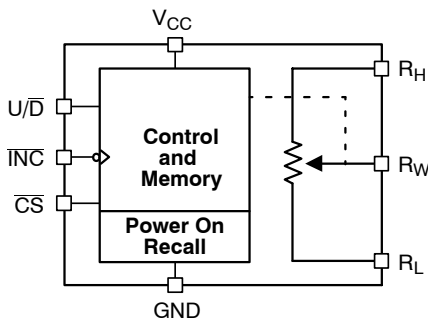


Figure 1. General

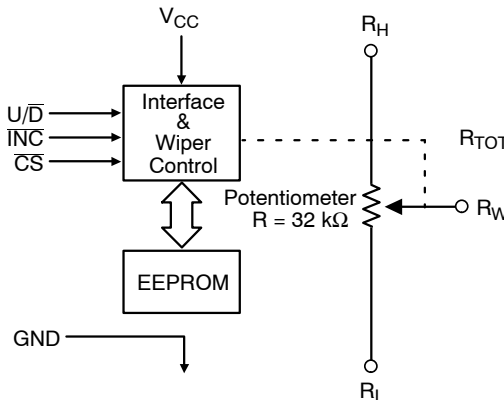


Figure 2. Block Diagram

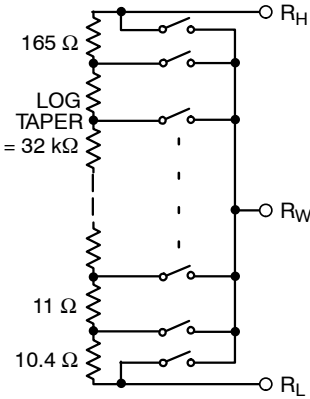


Figure 3. Potentiometer Schematic

Pin Description

**INC:** Increment Control Input

The **INC** input moves the wiper in the up or down direction determined by the condition of the **U/D** input.

**U/D:** Up/Down Control Input

The **U/D** input controls the direction of the wiper movement. When in a high state and **CS** is low, any high-to-low transition on **INC** will cause the wiper to move one increment toward the **R<sub>H</sub>** terminal. When in a low state and **CS** is low, any high-to-low transition on **INC** will cause the wiper to move one increment towards the **R<sub>L</sub>** terminal.

**R<sub>H</sub>:** High End Potentiometer Terminal

**R<sub>H</sub>** is the high end terminal of the potentiometer. It is not required that this terminal be connected to a potential greater than the **R<sub>L</sub>** terminal. Voltage applied to the **R<sub>H</sub>** terminal cannot exceed the supply voltage, **V<sub>CC</sub>** or go below ground, **GND**.

**R<sub>W</sub>:** Wiper Potentiometer Terminal

**R<sub>W</sub>** is the wiper terminal of the potentiometer. Its position on the resistor array is controlled by the control inputs, **INC**, **U/D** and **CS**. Voltage applied to the **R<sub>W</sub>** terminal cannot exceed the supply voltage, **V<sub>CC</sub>** or go below ground, **GND**.

**R<sub>L</sub>:** Low End Potentiometer Terminal

**R<sub>L</sub>** is the low end terminal of the potentiometer. It is not required that this terminal be connected to a potential less than the **R<sub>H</sub>** terminal. Voltage applied to the **R<sub>L</sub>** terminal cannot exceed the supply voltage, **V<sub>CC</sub>** or go below ground, **GND**. **R<sub>L</sub>** and **R<sub>H</sub>** are electrically interchangeable.

**CS:** Chip Select

The chip select input is used to activate the control input of the CAT5116 and is active low. When in a high state, activity on the **INC** and **U/D** inputs will not affect or change the position of the wiper.

Device Operation

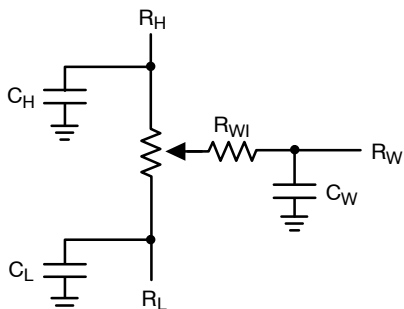
The CAT5116 operates like a digitally controlled potentiometer with **R<sub>H</sub>** and **R<sub>L</sub>** equivalent to the high and low terminals and **R<sub>W</sub>** equivalent to the mechanical potentiometer's wiper. There are 100 tap positions including the resistor end points, **R<sub>H</sub>** and **R<sub>L</sub>**. There are 99 resistor elements connected in series between the **R<sub>H</sub>** and **R<sub>L</sub>** terminals. The wiper terminal is connected to one of the 100 taps and controlled by three inputs, **INC**, **U/D** and **CS**. These inputs control a seven-bit up/down counter whose output is decoded to select the wiper position. The selected wiper position can be stored in nonvolatile memory using the **INC** and **CS** inputs.

With **CS** set LOW the CAT5116 is selected and will respond to the **U/D** and **INC** inputs. HIGH to LOW transitions on **INC** will increment or decrement the wiper (depending on the state of the **U/D** input and seven-bit counter). The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. The value of the counter is stored in nonvolatile memory whenever **CS** transitions HIGH while the **INC** input is also HIGH. When the CAT5116 is powered-down, the last stored wiper counter position is maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the counter is set to the value stored.

With **INC** set low, the CAT5116 may be deselected and powered down without storing the current wiper position in nonvolatile memory. This allows the system to always power up to a preset value stored in nonvolatile memory.

**Table 1. OPERATION MODES**

$\overline{\text{INC}}$	$\overline{\text{CS}}$	$\text{U}/\overline{\text{D}}$	Operation
High to Low	Low	High	Wiper toward H
High to Low	Low	Low	Wiper toward L
High	Low to High	X	Store Wiper Position
Low	Low to High	X	No Store, Return to Standby
X	High	X	Standby



**Figure 4. Potentiometer Equivalent Circuit**

**Table 2. ABSOLUTE MAXIMUM RATINGS**

Parameters	Ratings	Units
Supply Voltage $V_{CC}$ to GND	-0.5 to +7	V
Inputs $\overline{\text{CS}}$ to GND	-0.5 to $V_{CC} + 0.5$	V
$\overline{\text{INC}}$ to GND	-0.5 to $V_{CC} + 0.5$	V
$\text{U}/\overline{\text{D}}$ to GND	-0.5 to $V_{CC} + 0.5$	V
$R_H$ to GND	-0.5 to $V_{CC} + 0.5$	V
$R_L$ to GND	-0.5 to $V_{CC} + 0.5$	V
$R_W$ to GND	-0.5 to $V_{CC} + 0.5$	V
Operating Ambient Temperature Industrial ('I' suffix)	-40 to +85	°C
Junction Temperature (10 s)	+150	°C
Storage Temperature	+150	°C
Lead Soldering (10 s max)	+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Table 3. RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Test Method	Min	Typ	Max	Units
$V_{ZAP}$ (Note 1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			V
$I_{LTH}$ (Notes 1, 2)	Latch-Up	JEDEC Standard 17	100			mA
$T_{DR}$	Data Retention	MIL-STD-883, Test Method 1008	100			Years
$N_{END}$	Endurance	MIL-STD-883, Test Method 1003	1,000,000			Stores

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1 V to  $V_{CC} + 1$  V.

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**Table 4. DC ELECTRICAL CHARACTERISTICS** ( $V_{CC} = +2.5\text{ V}$  to  $+5.5\text{ V}$  unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>POWER SUPPLY</b>						
$V_{CC}$	Operating Voltage Range		2.5	–	5.5	V
$I_{CC1}$ (Note 5)	Supply Current (Increment)	$V_{CC} = 5.5\text{ V}$ , $f = 1\text{ MHz}$ , $I_W = 0$	–	–	100	$\mu\text{A}$
		$V_{CC} = 5.5\text{ V}$ , $f = 250\text{ kHz}$ , $I_W = 0$	–	–	50	$\mu\text{A}$
$I_{CC2}$	Supply Current (Write)	Programming, $V_{CC} = 5.5\text{ V}$	–	–	1	mA
		$V_{CC} = 3\text{ V}$	–	–	500	$\mu\text{A}$
$I_{SB1}$	Supply Current (Standby)	$\overline{CS} = V_{CC} - 0.3\text{ V}$ $U/\overline{D}$ , $\overline{INC} = V_{CC} - 0.3\text{ V}$ or GND	–	0.01	1	$\mu\text{A}$
<b>LOGIC INPUTS</b>						
$I_{IH}$	Input Leakage Current	$V_{IN} = V_{CC}$	–	–	10	$\mu\text{A}$
$I_{IL}$	Input Leakage Current	$V_{IN} = 0\text{ V}$	–	–	–10	$\mu\text{A}$
$V_{IH1}$	TTL High Level Input Voltage	$4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	2	–	$V_{CC}$	V
$V_{IL1}$	TTL Low Level Input Voltage		0	–	0.8	V
$V_{IH2}$	CMOS High Level Input Voltage	$2.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$	$V_{CC} \times 0.7$	–	$V_{CC} + 0.3$	V
$V_{IL2}$	CMOS Low Level Input Voltage		–0.3	–	$V_{CC} \times 0.2$	V
<b>POTENTIOMETER PARAMETERS</b>						
$R_{POT}$	Potentiometer Resistance			32		k $\Omega$
$R_{TOL}$	Pot. Resistance Tolerance				$\pm 20$	%
$V_{RH}$	Voltage on $R_H$ pin		0		$V_{CC}$	V
$V_{RL}$	Voltage on $R_L$ pin		0		$V_{CC}$	V
$R_V$ (Note 6)	Relative Variation				0.05	
$R_{WI}$	Wiper Resistance	$V_{CC} = 5\text{ V}$ , $I_W = 1\text{ mA}$		200	400	$\Omega$
		$V_{CC} = 2.5\text{ V}$ , $I_W = 1\text{ mA}$		400	1000	$\Omega$
$I_W$	Wiper Current				1	mA
$TC_{RPOT}$	TC of Pot Resistance			300		ppm/ $^{\circ}\text{C}$
$TC_{RATIO}$	Ratiometric TC				20	ppm/ $^{\circ}\text{C}$
$V_N$	Noise	100 kHz / 1 kHz		8/24		nV/ $\sqrt{\text{Hz}}$
$C_H/C_L/C_W$	Potentiometer Capacitances			8/8/25		pF
$f_c$	Frequency Response	Passive Attenuator, 10 k $\Omega$		1.7		MHz

3. Latch-up protection is provided for stresses up to 100 mA on address and data pins from  $-1\text{ V}$  to  $V_{CC} + 1\text{ V}$ .
4. This parameter is tested initially and after a design or process change that affects the parameter.
5.  $I_W$  = source or sink.
6. Relative variation is a measure of the error in step size between taps =  $\log(V_{W(N)}) - \log(V_{W(N-1)}) = 0.045 \pm 0.003$ .

**Table 5. AC TEST CONDITIONS**

V <sub>CC</sub> Range	2.5 V ≤ V <sub>CC</sub> ≤ 5.5 V
Input Pulse Levels	0.2 V <sub>CC</sub> to 0.7 V <sub>CC</sub>
Input Rise and Fall Times	10 ns
Input Reference Levels	0.5 V <sub>CC</sub>

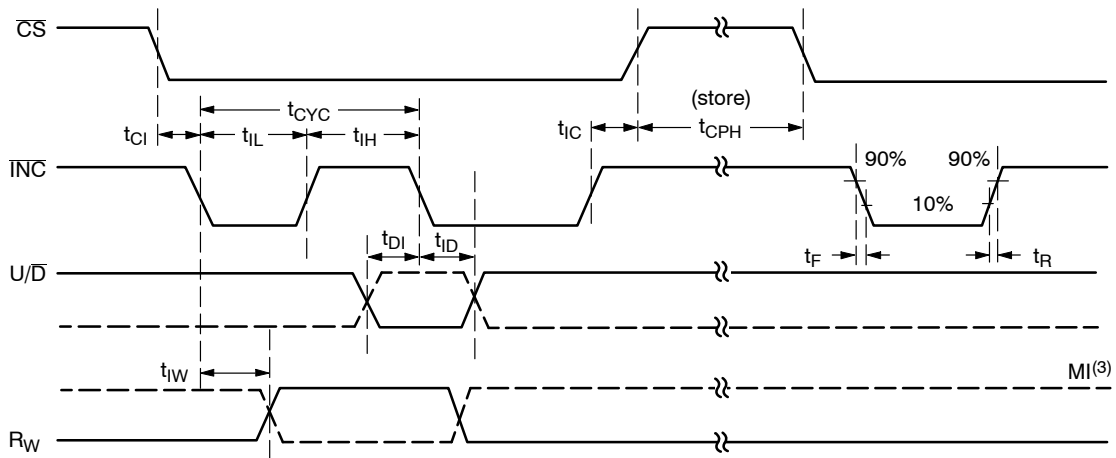
**Table 6. AC OPERATING CHARACTERISTICS** (V<sub>CC</sub> = +2.5 V to +5.5 V, V<sub>H</sub> = V<sub>CC</sub>, V<sub>L</sub> = 0 V, unless otherwise specified)

Symbol	Parameter	Min	Typ (Note 7)	Max	Units
t <sub>CI</sub>	$\overline{CS}$ to $\overline{INC}$ Setup	100	-	-	ns
t <sub>DI</sub>	U/ $\overline{D}$ to $\overline{INC}$ Setup	50	-	-	ns
t <sub>ID</sub>	U/ $\overline{D}$ to $\overline{INC}$ Hold	100	-	-	ns
t <sub>IL</sub>	$\overline{INC}$ LOW Period	250	-	-	ns
t <sub>IH</sub>	$\overline{INC}$ HIGH Period	250	-	-	ns
t <sub>IC</sub>	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1	-	-	μs
t <sub>CPH1</sub>	$\overline{CS}$ Deselect Time (NO STORE)	100	-	-	ns
t <sub>CPH2</sub>	$\overline{CS}$ Deselect Time (STORE)	10	-	-	ms
t <sub>IW</sub>	$\overline{INC}$ to V <sub>OUT</sub> Change	-	1	5	μs
t <sub>CYC</sub>	$\overline{INC}$ Cycle Time	1	-	-	μs
t <sub>R</sub> , t <sub>F</sub> (Note 8)	$\overline{INC}$ Input Rise and Fall Time	-	-	500	μs
t <sub>PU</sub> (Note 8)	Power-up to Wiper Stable	-	-	1	ms
t <sub>WR</sub>	Store Cycle	-	5	10	ms

7. Typical values are for T<sub>A</sub> = 25°C and nominal supply voltage.

8. This parameter is periodically sampled and not 100% tested.

9. MI in the A.C. Timing diagram refers to the minimum incremental change in the W output due to a change in the wiper position.



**Figure 5. A.C. Timing**

TYPICAL CHARACTERISTICS

( $V_{CC} = 5\text{ V}$ ,  $T_{AMB} = 25^\circ\text{C}$ , unless otherwise specified)

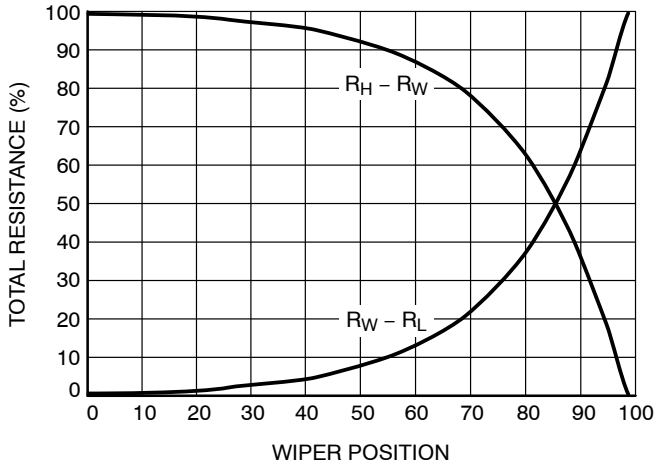


Figure 6. Wiper-Low/High Resistances vs. Wiper Position

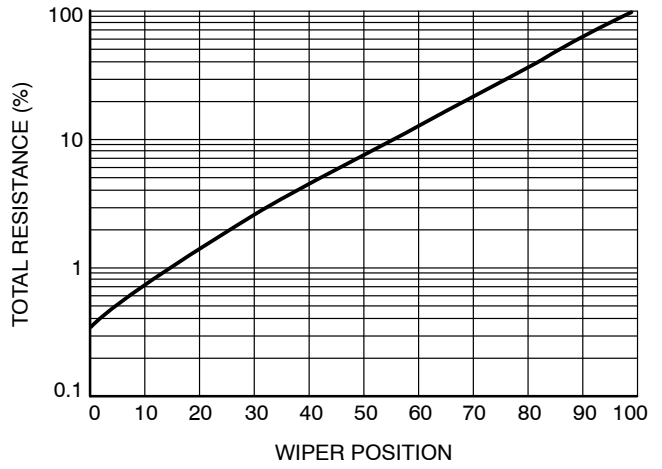


Figure 7. Wiper-Low Resistance vs. Wiper Position (Log Scale)

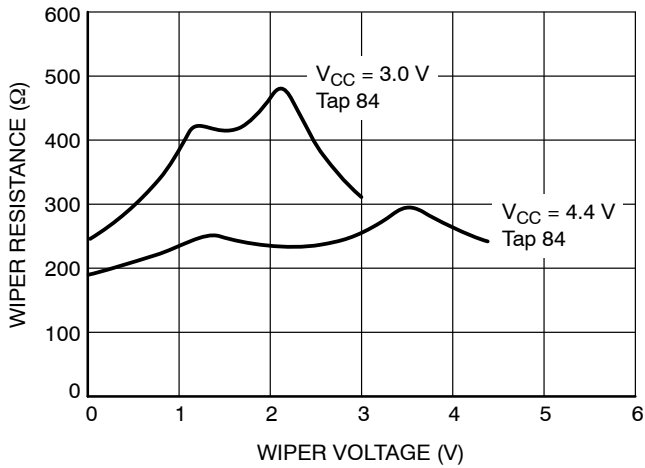


Figure 8. Wiper Resistance vs. Wiper Voltage

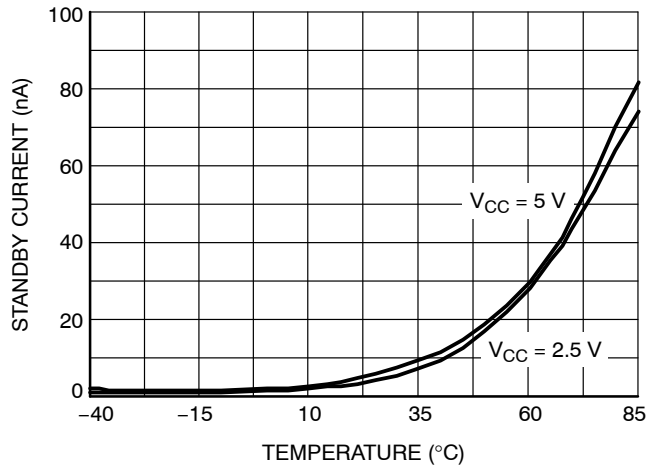


Figure 9. Standby Supply Current vs. Temperature

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**Table 7. ORDERING INFORMATION**

Device	Package	Shipping
CAT5116LI-G	PDIP-8 (Pb-Free)	100 Units / Rail
CAT5116VI-G	SOIC-8 (Pb-Free)	100 Units / Rail
CAT5116VI-GT3	SOIC-8 (Pb-Free)	3000 / Tape & Reel
CAT5116YI-G	TSSOP-8 (Pb-Free)	100 Units / Rail
CAT5116YI-GT3	TSSOP-8 (Pb-Free)	3000 / Tape & Reel
CAT5116ZI	MSOP-8 (Pb-Free)	96 Units / Rail
CAT5116ZI-T3	MSOP-8 (Pb-Free)	3000 / Tape & Reel

10. All packages are RoHS-compliant (Lead-free, Halogen-free).

11. The standard lead finish is NiPdAu.

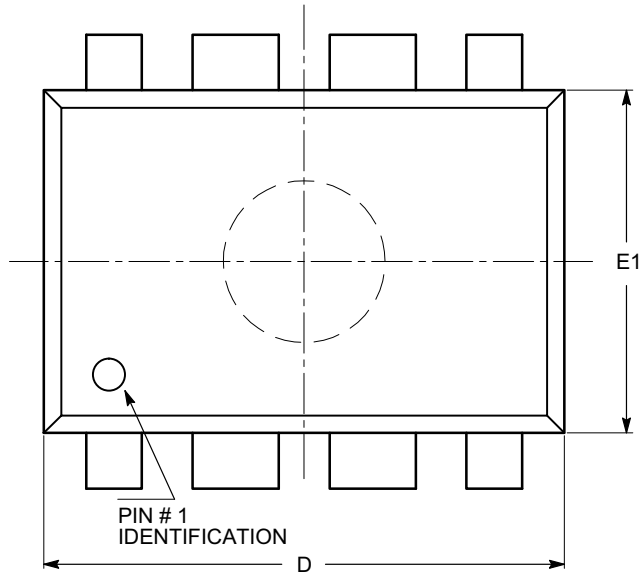
12. Contact factory for Matte-Tin finish.

13. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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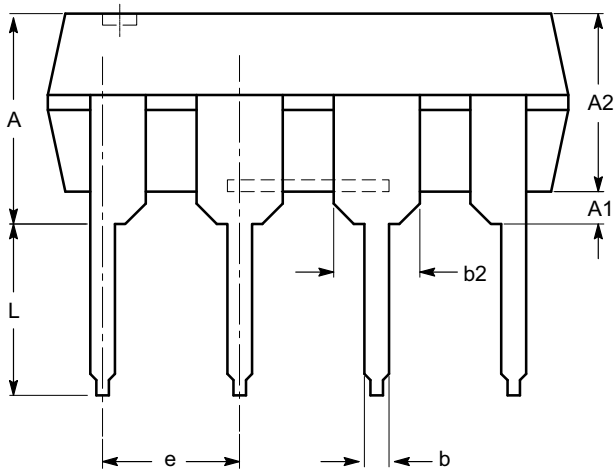
## PACKAGE DIMENSIONS

PDIP-8, 300 mils  
CASE 646AA-01  
ISSUE A

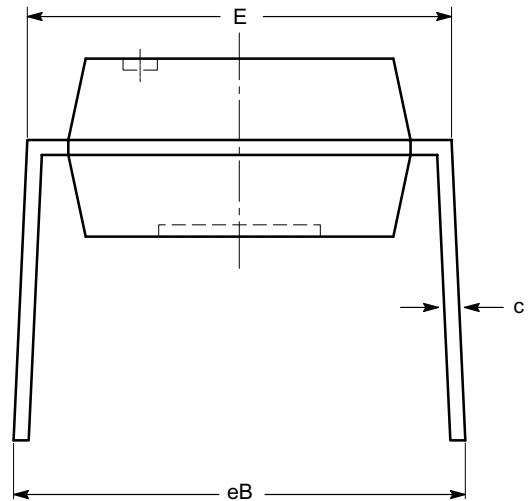


SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e	2.54 BSC		
eB	7.87		10.92
L	2.92	3.30	3.80

TOP VIEW



SIDE VIEW



END VIEW

**Notes:**

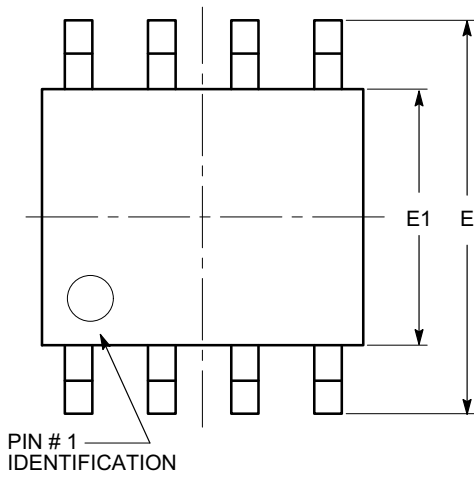
- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.



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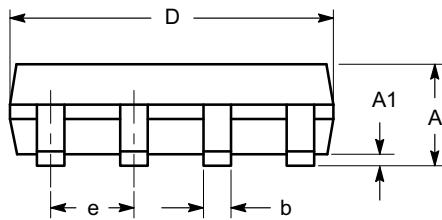
## PACKAGE DIMENSIONS

SOIC 8, 150 mils  
CASE 751BD-01  
ISSUE O

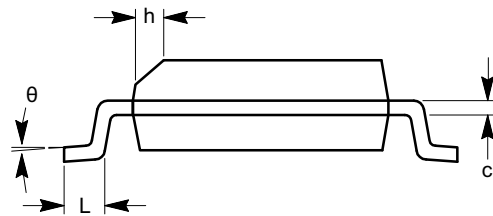


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
$\theta$	0°		8°



SIDE VIEW



END VIEW

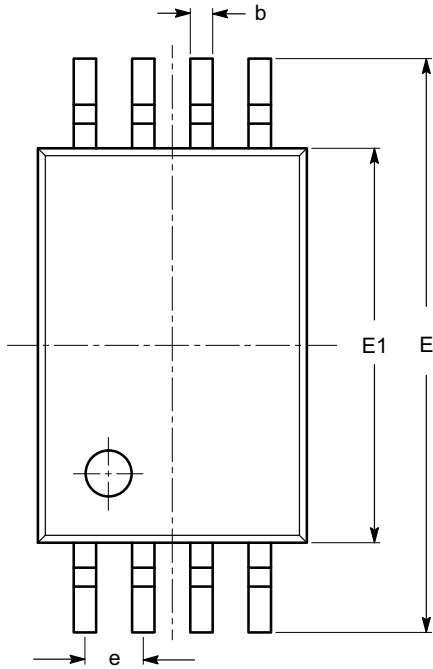
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

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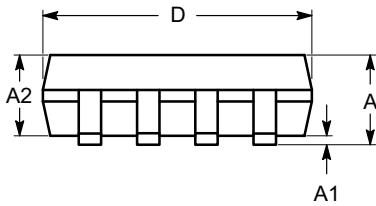
## PACKAGE DIMENSIONS

TSSOP8, 4.4x3  
CASE 948AL-01  
ISSUE O

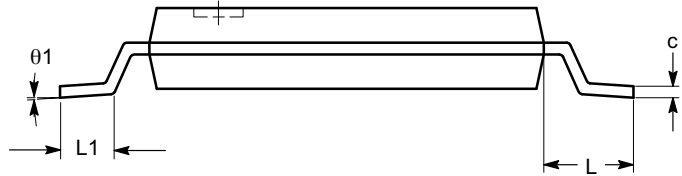


SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta$	0°		8°

TOP VIEW



SIDE VIEW



END VIEW

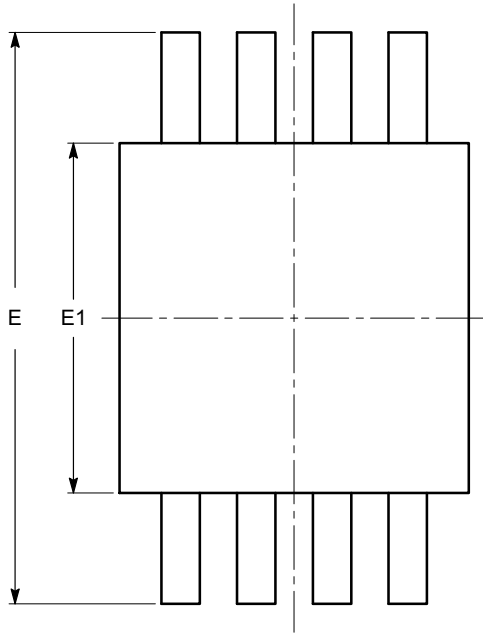
**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

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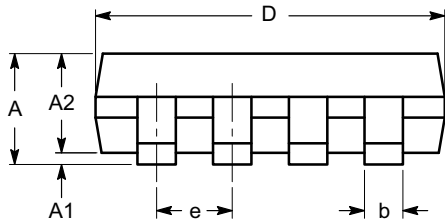
## PACKAGE DIMENSIONS

MSOP 8, 3x3  
CASE 846AD-01  
ISSUE O

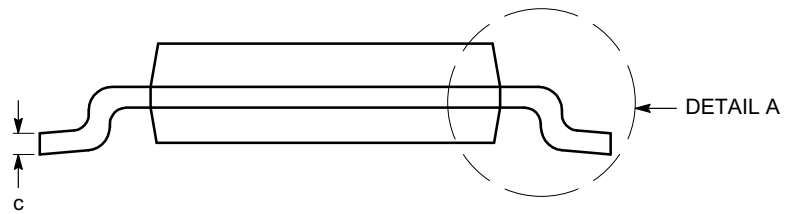


TOP VIEW

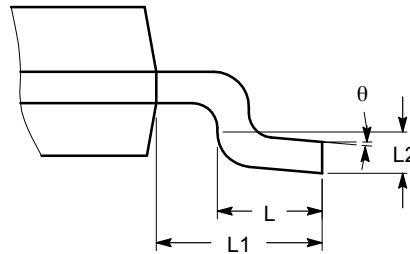
SYMBOL	MIN	NOM	MAX
A			1.10
A1	0.05	0.10	0.15
A2	0.75	0.85	0.95
b	0.22		0.38
c	0.13		0.23
D	2.90	3.00	3.10
E	4.80	4.90	5.00
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.40	0.60	0.80
L1	0.95 REF		
L2	0.25 BSC		
$\theta$	0°		6°



SIDE VIEW




END VIEW



DETAIL A

**Notes:**

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-187.

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