National Semiconductor

CD4021BM/CD4021BC 8-Stage Static Shift Register

General Description

The CD4021BM/CD4021BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q output are available from the sixth, seventh, and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is jammed into each stage of the register asynchronously with the clock.

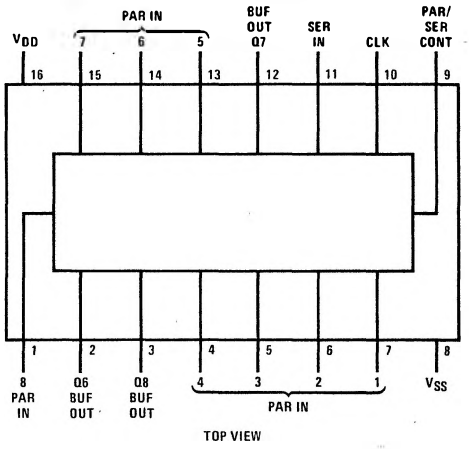
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagram

Dual-In-Line Package



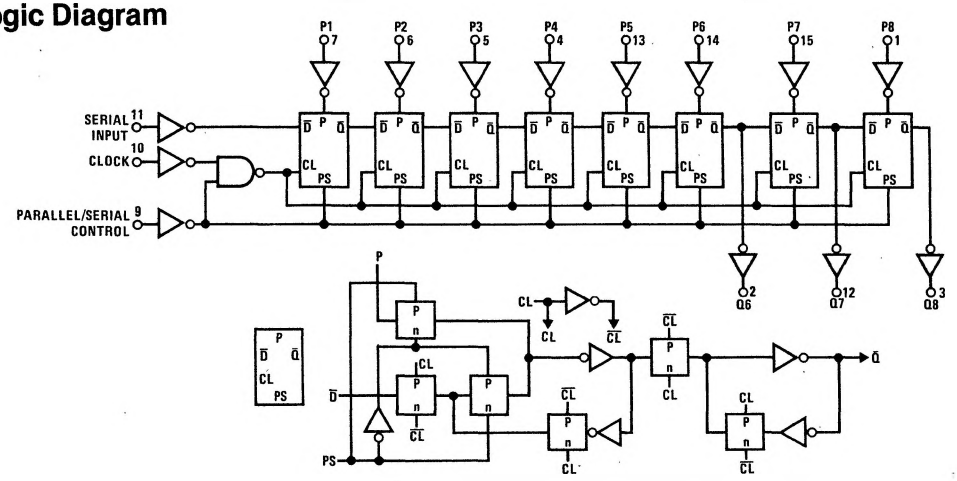
TOP VIEW

Truth Table

CL*	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌒	0	0	X	X	0	Q_{n-1}	
⌒	1	0	X	X	1	Q_{n-1}	
⌒	X	0	X	X	Q1	Q_n	No Change

*Level change
X = Don't care case

Logic Diagram



Absolute Maximum Ratings (Notes 1 & 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4021BM	−55°C to +125°C
CD4021BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4021BM

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		5		0.1	5		150	μA
		$V_{DD}=10V$		10		0.2	10		300	μA
		$V_{DD}=15V$		20		0.3	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$ | $\|I_O\|<1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$ | $\|I_O\|<1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$ | $\|I_O\|<1\mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$ | $\|I_O\|<1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4021BC

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		20		0.1	20		150	μA
		$V_{DD}=10V$		40		0.2	40		300	μA
		$V_{DD}=15V$		80		0.3	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$ | $\|I_O\|<1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$ | $\|I_O\|<1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$ | $\|I_O\|<1\mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$ | $\|I_O\|<1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD}=5V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

Parameter		Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		240	350	ns
		$V_{DD} = 10V$		100	175	ns
		$V_{DD} = 15V$		70	140	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	2.5	3.5		MHz
		$V_{DD} = 10V$	5	10		MHz
		$V_{DD} = 15V$	8	16		MHz
t_W	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_rCL, t_fCL	Clock Rise and Fall Time (Note 3)	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			15	μs
		$V_{DD} = 15V$			15	μs
t_s	Minimum Set-up Time					
	Serial Input	$V_{DD} = 5V$		60	120	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		40	80	ns
	(Ref. to CL)	$V_{DD} = 15V$		30	60	ns
	Parallel Inputs	$V_{DD} = 5V$		25	50	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		15	30	ns
	(Ref. to P/S)	$V_{DD} = 15V$		10	20	ns
t_H	Minimum Hold Time	$V_{DD} = 5V$			0	ns
	Serial In, Parallel In, $t_s \geq 400$ ns	$V_{DD} = 10V$			10	ns
	Parallel/Serial Control	$V_{DD} = 15V$			15	ns
t_{WH}	Minimum P/S Pulse Width	$V_{DD} = 5V$		150	250	ns
		$V_{DD} = 10V$		75	125	ns
		$V_{DD} = 15V$		50	100	ns
t_{REM}	Minimum P/S Removal Time	$V_{DD} = 5V$		100	200	ns
	(Ref. to CL)	$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)			100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: If more than one unit is cascaded t_rCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Typical Performance Characteristics