4Mb Late Write LVTTL High Speed Synchronous SRAM (256K x 18 Organization)

## Description

The CXK77B1841 is a high speed BiCMOS synchronous static RAM with common I/O pins, organized as 262,144-words by 18-bits. This synchronous SRAM integrates input registers, high speed RAM, output registers/latches, and a one-deep write buffer onto a single monolithic IC. Three different read protocols - Register-Register (R-R), Register-Latch (R-L), and Register-Flow Thru (R-FT), and an enhanced write protocol - Late (Delayed) Write (LW), are supported, providing a flexible, high-performance user interface.

All input signals except $\overline{G}$ (Output Enable) and ZZ (Sleep Mode) are registered on the positive edge of K clock.

Read cycles can be controlled in one of three ways - with registered outputs in Register-Register mode, with latched outputs in Register-Latch mode, or with flow-through outputs in Register-Flow Thru mode. The read protocol is user-selectable through external mode pins M1 and M2.

Write cycles follow a Late Write protocol, where data is provided to the SRAM one clock cycle after the address and control signals, eliminating one dead cycle from Read-to-Write transitions. In this scheme, when a write cycle is initiated, the address and data stored in the SRAM's write buffer during the previous write cycle are directed to the SRAM's memory core, while, simultaneously, the address and data from the current write cycle are stored in the SRAM's write buffer. In both Register-Latch and Register-Flow Thru modes, when $\overline{SW}$ (Global Write Enable) is driven active, the subsequent positive edge of K clock tri-states the SRAM's output drivers immediately, allowing consecutive Read-Write-Read operations. The write cycle is internally self-timed, which eliminates complex off-chip write pulse generation and provides increased flexibility for incoming signals.

Sleep (power down) mode control is provided through the asynchronous ZZ input. 220 MHz operation is obtained from a single 3.3V power supply. JTAG boundary scan interface is provided using a subset of IEEE standard 1149.1 protocol.

## Features

| | | R-R Mode | R-L, R-FT Modes |
|---|---|---|---|
| • Fast Cycle/Access Time | | $t_{KHKH}$ / $t_{KHQV}$ | $t_{KHKH}$ / $t_{KHQV}$ |
| CXK77B1841 | -45 | 4.5ns / 2.4ns | 5.5ns / 5.5ns |
| | -5 (*) | 5.0ns / 2.5ns | 5.7ns / 5.7ns |
| | -6 | 6.0ns / 3.0ns | 6.0ns / 6.0ns |

Note (*): Contact Sony Memory Marketing for availability of "-5" speed bin.

- 3 synchronous modes of operation, selectable by mode pins:
  Register-Register; Register-Latch; Register-Flow Thru;
- Single +3.3V power supply: 3.3V ± 5%
- Dedicated output supply voltage: $V_{DDQ}$ (2.5V to 3.3V typical)
- Inputs and outputs are LVTTL/LVCMOS compatible.
- Differential clock input (K/$\overline{K}$). Clock levels are compatible to PECL, LVTTL and LVCMOS.
- All inputs (except asynchronous $\overline{G}$ and ZZ) and outputs are registered on a single clock edge.
- Byte Write capability.
- Late Write scheme to eliminate one dead cycle from Read-to-Write transitions.
- Self-timed write cycles.
- Sleep (power down) mode.
- JTAG boundary scan (subset of IEEE standard 1149.1).
- 119 pin (7x17) Plastic Ball Grid Array (PBGA) package.

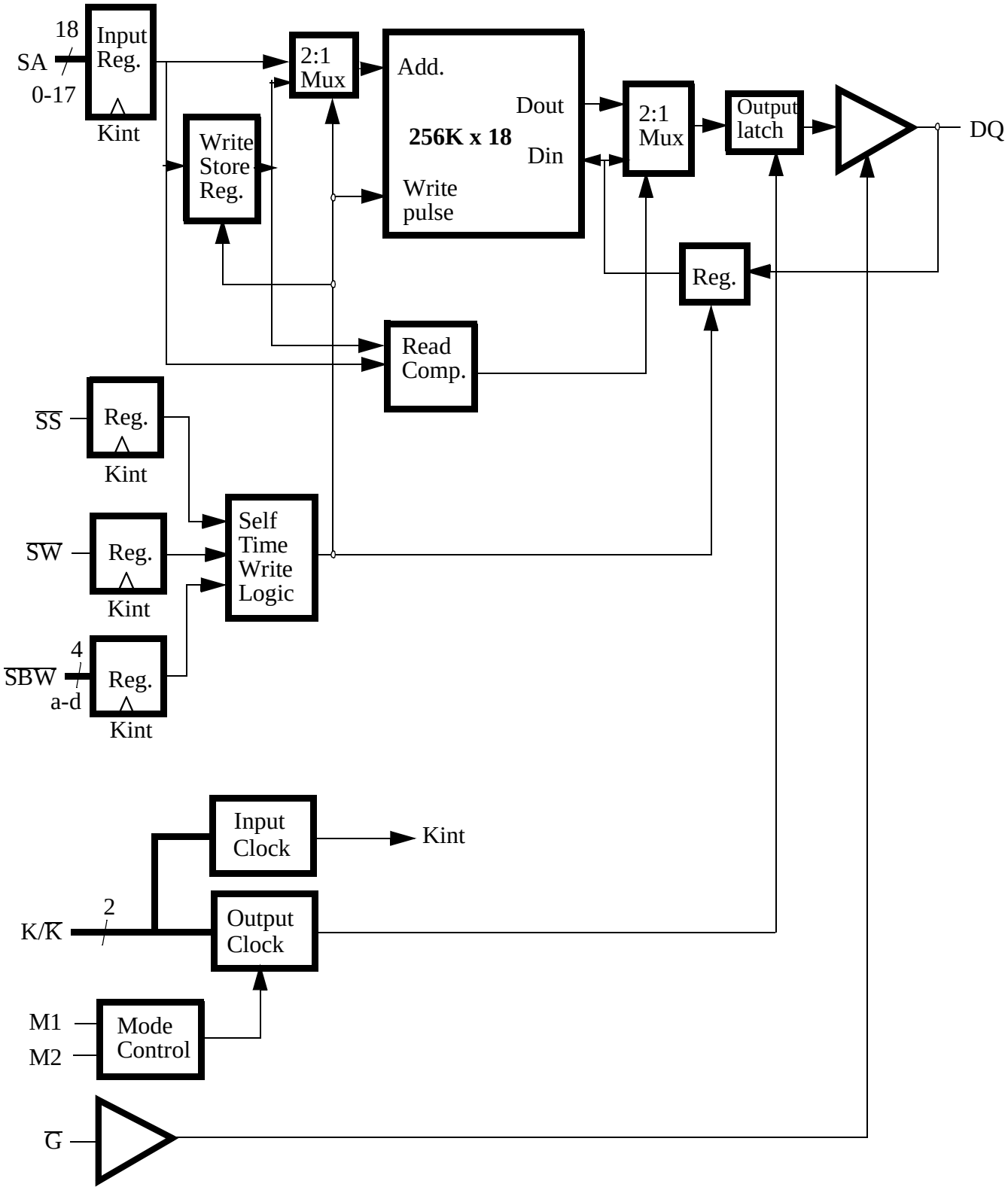
## Pin Configuration (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| A | $V_{DDQ}$ | SA6 | SA7 | NC | SA3 | SA2 | $V_{DDQ}$ |
| B | NC | NC | SA8 | NC | SA4 | NC | NC |
| C | NC | SA12 | SA5 | $V_{DD}$ | SA0 | SA13 | NC |
| D | DQ0b | NC | $V_{SS}$ | NC | $V_{SS}$ | DQ8a | NC |
| E | NC | DQ1b | $V_{SS}$ | $\overline{SS}$ | $V_{SS}$ | NC | DQ7a |
| F | $V_{DDQ}$ | NC | $V_{SS}$ | $\overline{G}$ | $V_{SS}$ | DQ6a | $V_{DDQ}$ |
| G | NC | DQ2b | $\overline{SBW}$b | $\overline{C}$ | $V_{SS}$ | NC | DQ5a |
| H | DQ3b | NC | $V_{SS}$ | C | $V_{SS}$ | DQ4a | NC |
| J | $V_{DDQ}$ | $V_{DD}$ | NC | $V_{DD}$ | NC | $V_{DD}$ | $V_{DDQ}$ |
| K | NC | DQ4b | $V_{SS}$ | K | $V_{SS}$ | NC | DQ3a |
| L | DQ5b | NC | $V_{SS}$ | $\overline{K}$ | $\overline{SBW}$a | DQ2a | NC |
| M | $V_{DDQ}$ | DQ6b | $V_{SS}$ | $\overline{SW}$ | $V_{SS}$ | NC | $V_{DDQ}$ |
| N | DQ7b | NC | $V_{SS}$ | SA14 | $V_{SS}$ | DQ1a | NC |
| P | NC | DQ8b | $V_{SS}$ | SA11 | $V_{SS}$ | NC | DQ0a |
| R | NC | SA10 | M1 | $V_{DD}$ | M2 | SA15 | NC |
| T | NC | SA17 | SA9 | NC | SA1 | SA16 | ZZ |
| U | $V_{DDQ}$ | TMS | TDI | TCK | TDO | NC | $V_{DDQ}$ |

## Pin Description

| Symbol | Description | Symbol | Description | Symbol | Description |
|---|---|---|---|---|---|
| SA | Address Input (0-17) | $\overline{G}$ | Async. Output Enable | $V_{DDQ}$ | Output Power Supply |
| DQ | Data I/O (0-8), Bytes a,b | ZZ | Async. Sleep Mode | $V_{SS}$ | Ground |
| K,$\overline{K}$ | Differential Input Clocks | TCK | JTAG Clock (LVTTL) | M1,M2 | Mode Select |
| C,$\overline{C}$ | Differential Output Control Clocks (for future use) | TMS | JTAG Mode Select (LVTTL) | NC | No Connect |
| $\overline{SW}$ | Write Enable, Global | TDI | JTAG Data In (LVTTL) | | |
| $\overline{SBW}$x | Write Enable, Bytes a,b | TDO | JTAG Data Out (LVTTL) | | |
| $\overline{SS}$ | Synchronous Select | $V_{DD}$ | +3.3V Power Supply | | |

# BLOCK DIAGRAM



## •Truth Tables

### Register - Register Mode

| ZZ | $\overline{SS}$ ($t_n$) | $\overline{SW}$ ($t_n$) | $\overline{SBW}$x ($t_n$) | $\overline{G}$ | Mode | $DQ_{0-17}$ ($t_n$) | $DQ_{0-17}$ ($t_{n+1}$) | $V_{DD}$ Current |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Sleep Mode. Power Down | Hi - Z | Hi - Z | $I_{SB}$ |
| L | H | X | X | X | Deselect | X | Hi - Z | $I_{DD}$ |
| L | L | H | X | H | Read | Hi - Z | Hi - Z | $I_{DD}$ |
| L | L | H | X | L | Read | X | $Q(t_n)$ | $I_{DD}$ |
| L | L | L | L | X | Write All Bytes (Bits 0-17) | X | $D(t_n)$ | $I_{DD}$ |
| L | L | L | X | X | Write Bytes With $\overline{SBW}$x=L | X | $D(t_n)$ | $I_{DD}$ |
| L | L | L | H | X | Abort Write | X | Hi - Z | $I_{DD}$ |

### Register - Latch and Register - Flow Thru Mode

| ZZ | $\overline{SS}$ ($t_n$) | $\overline{SW}$ ($t_n$) | $\overline{SBW}$x ($t_n$) | $\overline{G}$ | Mode | $DQ_{0-17}$ ($t_n$) | $DQ_{0-17}$ ($t_{n+1}$) | $V_{DD}$ Current |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | Sleep Mode. Power Down | Hi - Z | Hi - Z | $I_{SB}$ |
| L | H | X | X | X | Deselect | Hi - Z | X | $I_{DD}$ |
| L | L | H | X | H | Read | Hi - Z | Hi - Z | $I_{DD}$ |
| L | L | H | X | L | Read | $Q(t_n)$ | X | $I_{DD}$ |
| L | L | L | L | X | Write All Bytes (Bits 0-17) | Hi - Z | $D(t_n)$ | $I_{DD}$ |
| L | L | L | X | X | Write Bytes With $\overline{SBW}$x=L | Hi - Z | $D(t_n)$ | $I_{DD}$ |
| L | L | L | H | X | Abort Write | Hi - Z | X | $I_{DD}$ |

## •Mode Select

This device supports three different JEDEC standard read protocols via mode pins M1 and M2. The mode pins must be set during power-up and cannot change during SRAM operation.

**Mode Select Truth Table.**

| | M1 | M2 |
|---|---|---|
| Register-Register | L | H |
| Register-Flow Thru | L | L |
| Register-Latch | H | L |

## •Power-Up Sequence

Power supplies must power up in the following sequence: $V_{SS}$, $V_{DD}$, $V_{DDQ}$, and Inputs. $V_{DDQ}$ must never exceed $V_{DD}$.

## •Absolute Maximum Ratings(1)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | -0.5 to +4.6 | V |
| Output Supply Voltage | $V_{DDQ}$ | -0.5 to +4.6 | V |
| Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 (4.6V max.) | V |
| Output Voltage | $V_{OUT}$ | -0.5 to $V_{DDQ}$+0.5 (4.6V max.) | V |
| Operating Temperature | $T_A$ | 0 to 70 | °C |
| Junction Temperature | $T_J$ | 0 to 110 | °C |
| Storage Temperature | $T_{stg}$ | -55 to 150 | °C |

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions other than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## • DC Recommended Operating Conditions

**($V_{SS}$ = 0V, $T_A$ = 0 to 70°C)**

| Item | | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Supply Voltage | | | $V_{DD}$ | 3.13 | 3.3 | 3.47 | V |
| Output Supply Voltage(1) | | | $V_{DDQ}$ | 2.37 | 2.5, 3.3 | 3.47 | V |
| Address & Control | | Input High Voltage(2) | $V_{IHCA}$ | 1.65 | --- | $V_{DD}$ + 0.3 | V |
| | | Input Low Voltage(4) | $V_{ILCA}$ | -0.3 | --- | 1.15 | V |
| Data | | Input High Voltage(3) | $V_{IHD}$ | 1.65 | --- | $V_{DDQ}$ + 0.3 | V |
| | | Input Low Voltage(4) | $V_{ILD}$ | -0.3 | --- | 1.15 | V |
| Clock(5) | LVTTL | Input Signal Voltage | $V_{KIN}$ | -0.3 | --- | $V_{DD}$ + 0.3 | V |
| | | Input Differential Voltage | $V_{DIF}$ | 0.5 | --- | $V_{DD}$ + 0.6 | V |
| | | Input Common Mode Voltage | $V_{CM}$ | 1.15 | 1.4 | 1.75 | V |
| | | Input Cross Point Voltage | $V_X$ | 1.15 | 1.4 | 1.75 | V |
| | PECL | Input High Voltage | $V_{IH-PECL}$ | 2.135 | --- | 2.420 | V |
| | | Input Low Voltage | $V_{IL-PECL}$ | 1.480 | --- | 1.825 | V |

(1) For $V_{DDQ}$ = 2.5V or $V_{DDQ}$ = 3.3V application.
(2) $V_{IH}$ (Max) AC = $V_{DD}$+1.5 V for pulse width less than 2.0 ns
(3) $V_{IH}$ (Max) AC = $V_{DDQ}$+1.5 V for pulse width less than 2.0 ns
(4) $V_{IL}$ (Min) AC = -1.5 V for pulse width less than 2.0 ns.
(5) This device supports three different input clocking schemes:

a. LVTTL Differential - In this scheme, both clock inputs (K and $\overline{K}$) are driven differentially to the same voltage levels as the other inputs, i.e. from $V_{SS}$ to $V_{DDQ}$ nominally. $V_{KIN}$, $V_{DIF}$, and $V_{CM}$ must all be considered when using this scheme.

b. LVTTL Single Ended - In this scheme, one of the two clock inputs (either K or $\overline{K}$) is driven to the same voltage levels as the other inputs, i.e. from $V_{SS}$ to $V_{DDQ}$ nominally, while the other clock input (either $\overline{K}$ or K) is tied to an external reference voltage ($V_X$). $V_{KIN}$, $V_{DIF}$, and $V_X$ must all be considered when using this scheme.

c. PECL Differential - In this scheme, both clock inputs (K and $\overline{K}$) are driven differentially according to PECL guidelines. Both $V_{IH-PECL}$ and $V_{IL-PECL}$ must be considered when using this scheme.

## •I/O Capacitance

**($T_A$ = 25°C, f = 1 MHz)**

| Item | Symbol | Test conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$ = 0V | --- | 6 | pF |
| Clock Input Capacitance | $C_{CLK}$ | $V_{IN}$ = 0V | --- | 6 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$ = 0V | --- | 7 | pF |

Note: These parameters are sampled and are not 100% tested.

## •DC Electrical Characteristics

**($V_{DD}$ = 3.3V ± 5%, $V_{SS}$ = 0V, $T_A$ = 0 to 70°C)**

| Item | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI}$ | $V_{IN}$ = $V_{SS}$ to $V_{DD}$ | -1 | --- | 1 | uA |
| Output Leakage Current | $I_{LO}$ | $V_{OUT}$ = $V_{SS}$ to $V_{DD}$<br>$\overline{G}$ = $V_{IH}$ | -10 | --- | 10 | uA |
| Power Supply Operating Current | $I_{DD}$[1] | Cycle = 6.0ns<br>Duty = 100%<br>$I_{OUT}$ = 0 mA | --- | 600 | --- | mA |
| Power Supply Operating Current | $I_{DD}$[1] | Cycle = 5.5ns<br>Duty = 100%<br>$I_{OUT}$ = 0 mA | --- | 630 | --- | mA |
| Power Supply Operating Current | $I_{DD}$[1] | Cycle = 4.5ns<br>Duty = 100%<br>$I_{OUT}$ = 0 mA | --- | 685 | --- | mA |
| Power Supply Standby Current | $I_{SB}$ | ZZ ≥ $V_{IH}$ | --- | 60 | --- | mA |
| Output High Voltage $V_{DDQ}$ = 3.3V | $V_{OH}$ | $I_{OH}$ = -6.0 mA | 2.4 | --- | --- | V |
| Output Low Voltage $V_{DDQ}$ = 3.3V | $V_{OL}$ | $I_{OL}$ = 6.0 mA | --- | --- | 0.4 | V |
| Output High Voltage for $V_{DDQ}$ = 2.5V | $V_{OH}$ | $I_{OH}$ = -6.0 mA | 2.0 | --- | --- | V |
| Output Low Voltage for $V_{DDQ}$ = 2.5V | $V_{OL}$ | $I_{OL}$ = 6.0 mA | --- | --- | 0.4 | V |

1. Typical $I_{DD}$ values measured at $V_{DD}$ = 3.3V and $T_A$ = 25°C, with a 75% read / 25% write operation distribution.

## •AC Electrical Characteristics (Register-Register Mode)

| Item | Symbol | -45 | | -5 | | -6 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Cycle Time | $t_{KHKH}$ | 4.5 | --- | 5.0 | --- | 6.0 | --- | ns |
| Clock High Pulse Width | $t_{KHKL}$ | 1.5 | --- | 1.5 | --- | 2.0 | --- | ns |
| Clock Low Pulse Width | $t_{KLKH}$ | 1.5 | --- | 1.5 | --- | 2.0 | --- | ns |
| Address Setup Time | $t_{AVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Address Hold Time | $t_{KHAX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Write Enables Setup Time | $t_{WVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Write Enables Hold Time | $t_{KHWX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Synchronous Select Setup Time | $t_{SVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Synchronous Select Hold Time | $t_{KHSX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Data Input Setup Time | $t_{DVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Data Input Hold Time | $t_{KHDX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Clock High to Output Valid | $t_{KHQV}$ | --- | 2.4 | --- | 2.5 | --- | 3.0 | ns |
| Clock High to Output Hold | $t_{KHQX}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock High to Output Low-Z | $t_{KHQX1}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock High to Output High-Z ($\overline{SS}$ Deselect Cycle) | $t_{KHQZ}$ *2 | --- | 2.0 | --- | 2.0 | --- | 2.0 | ns |
| Output Enable Low to Output Valid | $t_{GLQV}$ | --- | 2.3 | --- | 2.5 | --- | 3.0 | ns |
| Output Enable Low to Output Low-Z | $t_{GLQX}$ *2 | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Output Enable High to Output High-Z | $t_{GHQZ}$ *2 | --- | 2.3 | --- | 2.5 | --- | 3.0 | ns |
| Sleep Mode Enable Time | $t_{ZZE}$ *2 | --- | 20.0 | --- | 20.0 | --- | 20.0 | ns |
| Sleep Mode Recovery Time | $t_{ZZR}$ *2 | 20.0 | --- | 20.0 | --- | 20.0 | | ns |

1. All parameters are specified over the range $T_A$ = 0 to 70°C.
2. These parameters are sampled and are not 100% tested.

## •AC Electrical Characteristics (Register-Latch & Register-Flow Thru Modes)

| Item | Symbol | -45 | | -5 | | -6 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Cycle Time | $t_{KHKH}$ | 5.5 | --- | 5.7 | --- | 6.0 | --- | ns |
| Clock High Pulse Width | $t_{KHKL}$ | 1.5 | --- | 1.5 | --- | 2.0 | --- | ns |
| Clock Low Pulse Width | $t_{KLKH}$ | 1.5 | --- | 1.5 | --- | 2.0 | --- | ns |
| Address Setup Time | $t_{AVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Address Hold Time | $t_{KHAX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Write Enables Setup Time | $t_{WVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Write Enables Hold Time | $t_{KHWX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Synchronous Select Setup Time | $t_{SVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Synchronous Select Hold Time | $t_{KHSX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Data Input Setup Time | $t_{DVKH}$ | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Data Input Hold Time | $t_{KHDX}$ | 1.0 | --- | 1.0 | --- | 1.0 | --- | ns |
| Clock High to Output Valid | $t_{KHQV}$ | --- | 5.5 | --- | 5.7 | --- | 6.0 | ns |
| Clock High to Output Hold (Flow Thru mode only) | $t_{KHQX}$ *2 | 2.0 | --- | 2.0 | --- | 2.0 | --- | ns |
| Clock High to Output Low-Z (Flow Thru mode only) | $t_{KHQX1}$ *2 | 2.0 | --- | 2.0 | --- | 3.0 | --- | ns |
| Clock Low to Output Valid (Latch mode only) | $t_{KLQV}$ | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| Clock Low to Output Hold (Latch mode only) | $t_{KLQX}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock Low to Output Low-Z (Latch mode only) | $t_{KLQX1}$ *2 | 0.7 | --- | 0.7 | --- | 0.7 | --- | ns |
| Clock High to Output High-Z ($\overline{SS}$ Deselect Cycle) | $t_{KHQZ}$ *2 | --- | 2.0 | --- | 2.0 | --- | 2.0 | ns |
| Clock High to Output High-Z ($\overline{SW}$ Write Cycle) | $t_{KHQZ1}$ *2 | --- | 2.0 | --- | 2.0 | --- | 2.0 | ns |
| Output Enable Low to Output Valid | $t_{GLQV}$ | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| Output Enable Low to Output Low-Z | $t_{GLQX}$ *2 | 0.5 | --- | 0.5 | --- | 0.5 | --- | ns |
| Output Enable High to Output High-Z | $t_{GHQZ}$ *2 | --- | 2.3 | --- | 2.5 | --- | 2.5 | ns |
| Sleep Mode Enable Time | $t_{ZZE}$ *2 | --- | 20.0 | --- | 20.0 | --- | 20.0 | ns |
| Sleep Mode Recovery Time | $t_{ZZR}$ *2 | 20.0 | --- | 20.0 | --- | 20.0 | | ns |

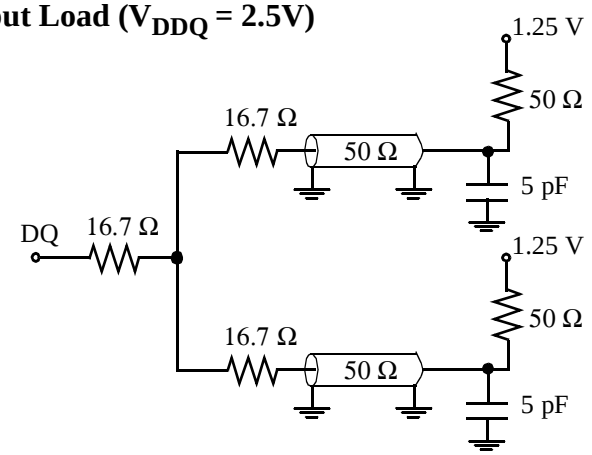
1. All parameters are specified over the range $T_A$ = 0 to 70°C.
2. These parameters are sampled and are not 100% tested.

## •AC Test Conditions ($V_{DDQ}$ = 2.5V)

**($V_{DD}$ = 3.3V ± 5%, $V_{DDQ}$ = 2.5V -5%/+10%, $T_A$ = 0 to 70°C)**

| Item | | Conditions | Notes |
|---|---|---|---|
| Address / Control / Data Input High Level | | $V_{IHCA}$, $V_{IHD}$ = 2.0V | @ Set up time ≥1ns |
| Address / Control / Data Input Low Level | | $V_{ILCA}$, $V_{ILD}$ = 0.8V | @ Set up time ≥1ns |
| Input Rise & Fall Time | | 1.0V/ns | Other than Clock |
| Input Reference Level | | 1.4V | Other than Clock |
| Clock | LVTTL Input High Voltage | 2.2V | $V_{DIF}$ ≥ 0.8V |
| | LVTTL Input Low Voltage | 0.6V | $V_{DIF}$ ≥ 0.8V |
| | LVTTL Input Common Mode Voltage | 1.4V | |
| | PECL Input High Voltage | $V_{IH-PECL}$ = 2.3V | |
| | PECL Input Low Voltage | $V_{IL-PECL}$ = 1.6V | |
| Clock Input Rise & Fall Time | | 1.0V/ns | |
| Clock Input Reference Level | | K/$\overline{K}$ cross | |
| Output Reference Level | | 1.25V | |
| Output Load Conditions | | | Fig.1 |

**Fig. 1: AC Test Output Load ($V_{DDQ}$ = 2.5V)**

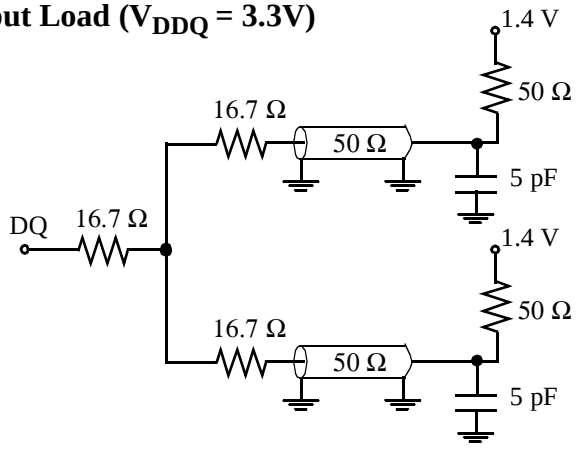


## •AC Test Conditions ($V_{DDQ}$ = 3.3V)

**($V_{DD}$ = $V_{DDQ}$ = 3.3V ± 5%, $T_A$ = 0 to 70°C)**

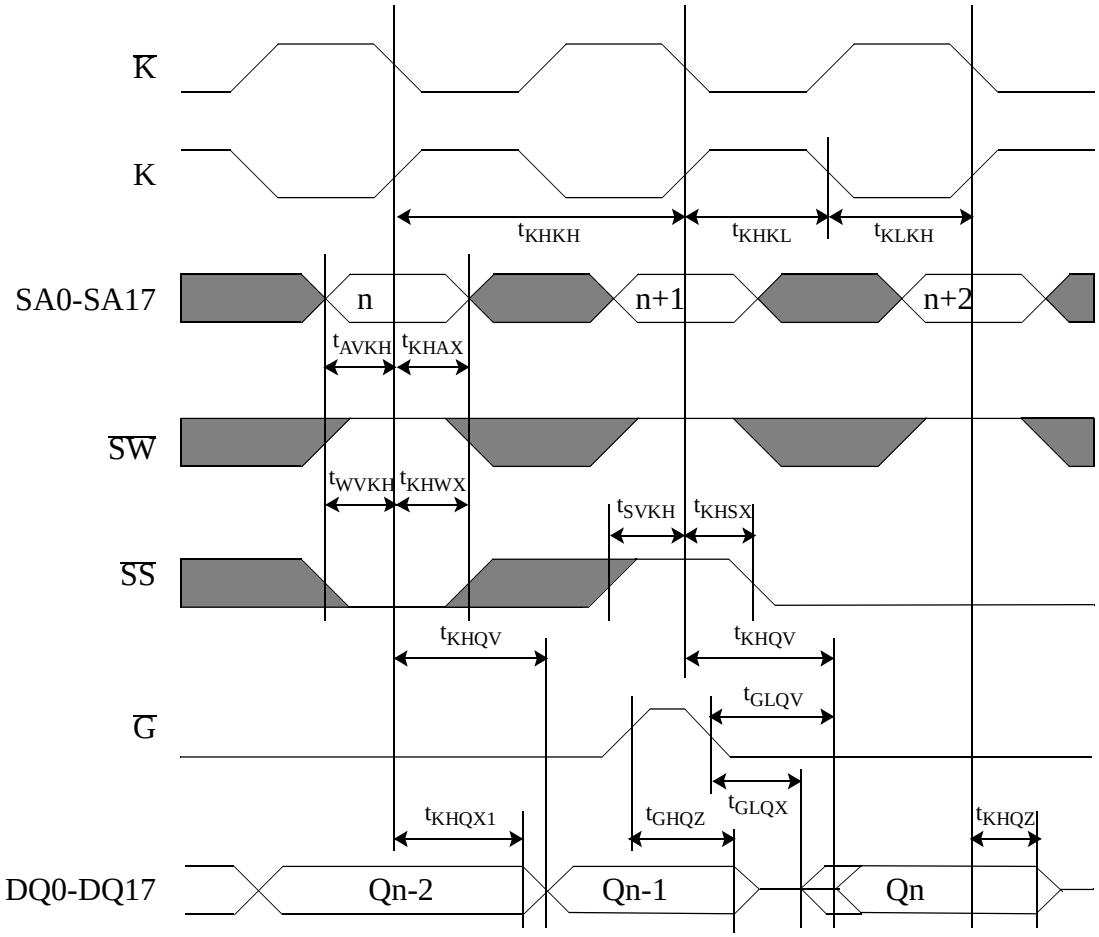
| Item | | Conditions | Notes |
|---|---|---|---|
| Address / Control / Data Input High Level | | $V_{IHCA}$, $V_{IHD}$ = 2.4V | @ Set up time ≥1ns |
| Address / Control / Data Input Low Level | | $V_{ILCA}$, $V_{ILD}$ = 0.4V | @ Set up time ≥1ns |
| Input Rise & Fall Time | | 1.0V/ns | Other than Clock |
| Input Reference Level | | 1.4V | Other than Clock |
| Clock | LVTTL Input High Voltage | 2.4V | $V_{DIF}$ ≥ 1.0V |
| | LVTTL Input Low Voltage | 0.4V | $V_{DIF}$ ≥ 1.0V |
| | LVTTL Input Common Mode Voltage | 1.4V | |
| | PECL Input High Voltage | $V_{IH-PECL}$ = 2.3V | |
| | PECL Input Low Voltage | $V_{IL-PECL}$ = 1.6V | |
| Clock Input Rise & Fall Time | | 1.0V/ns | |
| Clock Input Reference Level | | K/$\overline{K}$ cross | |
| Output Reference Level | | 1.4V | |
| Output Load Conditions | | | Fig.2 |

**Fig. 2: AC Test Output Load ($V_{DDQ}$ = 3.3V)**

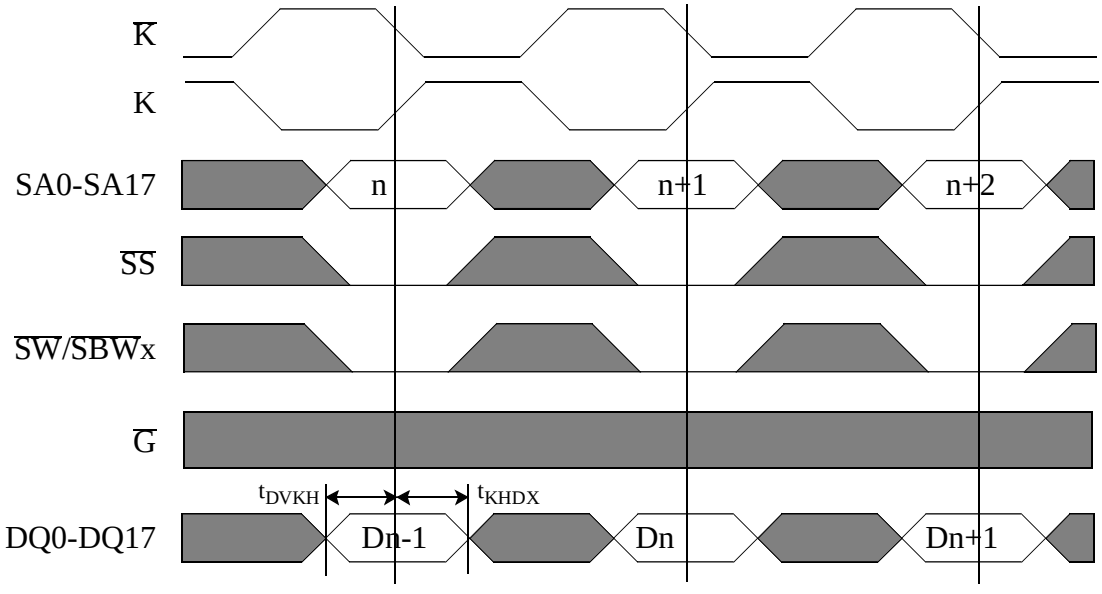


# Register - Register Mode

## TIMING WAVEFORM OF READ CYCLE

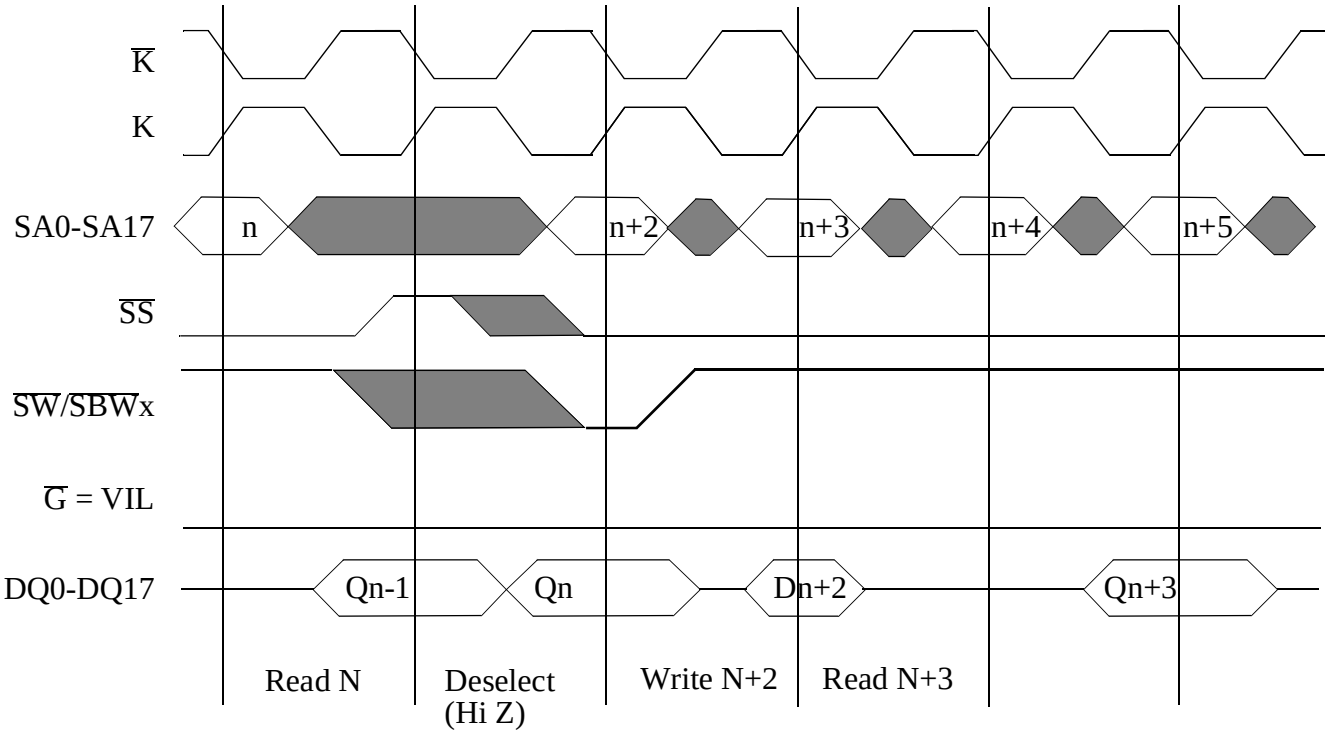



## TIMING WAVEFORM OF WRITE CYCLE

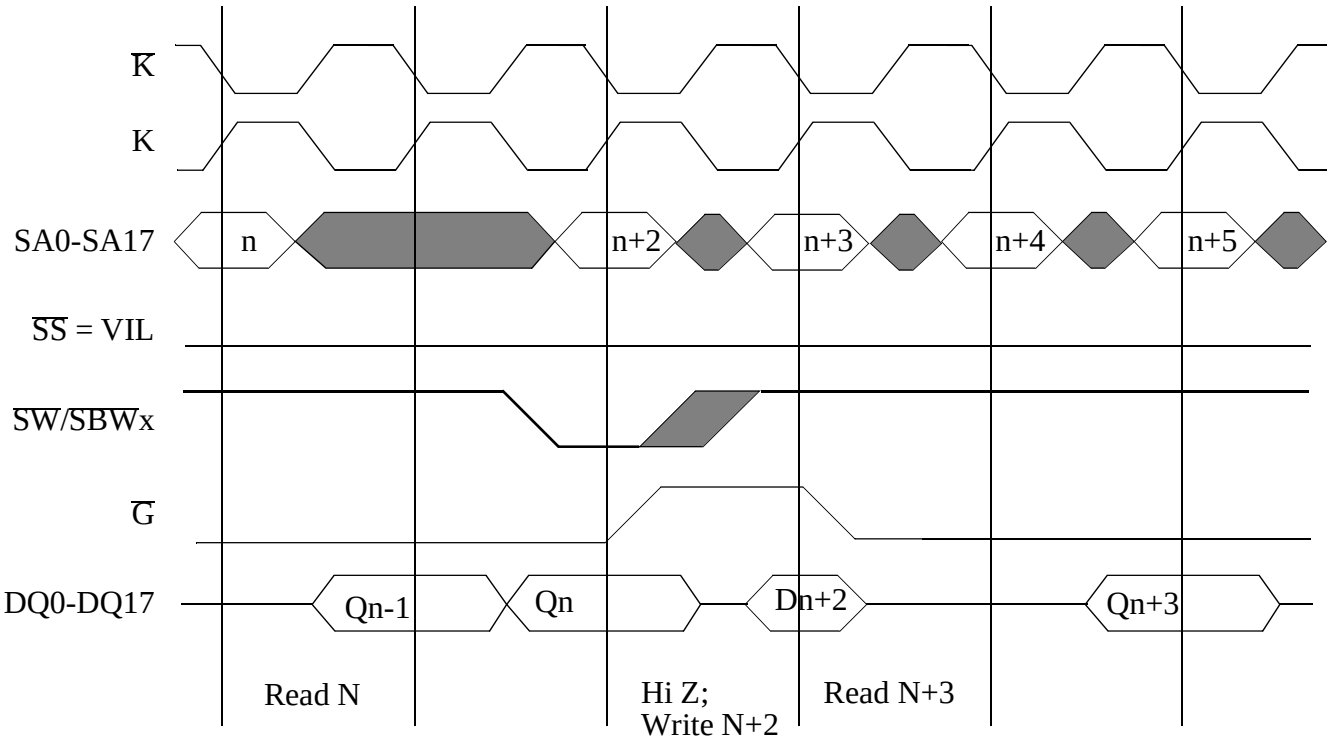


# Register - Register Mode

**TIMING WAVEFORM OF READ-WRITE-READ CYCLE I ($\overline{SS}$ controlled)**

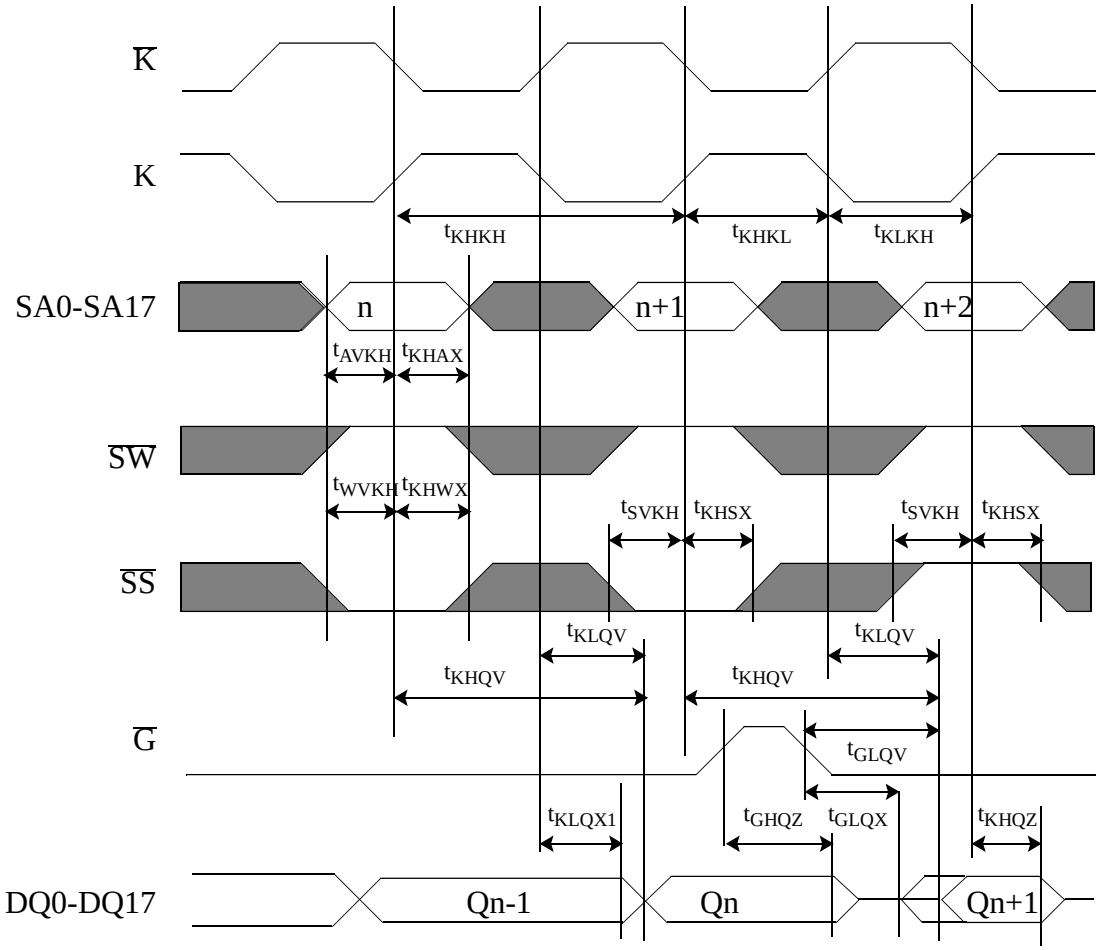



**TIMING WAVEFORM OF READ-WRITE-READ CYCLE II ($\overline{G}$ controlled)**

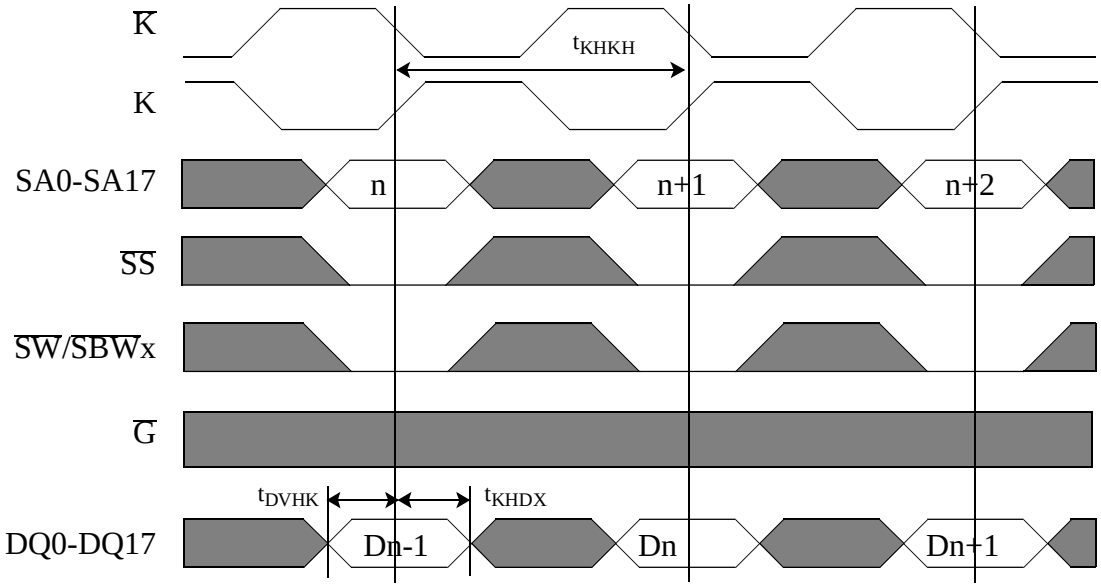


## Register - Latch Mode

### TIMING WAVEFORM OF READ CYCLE

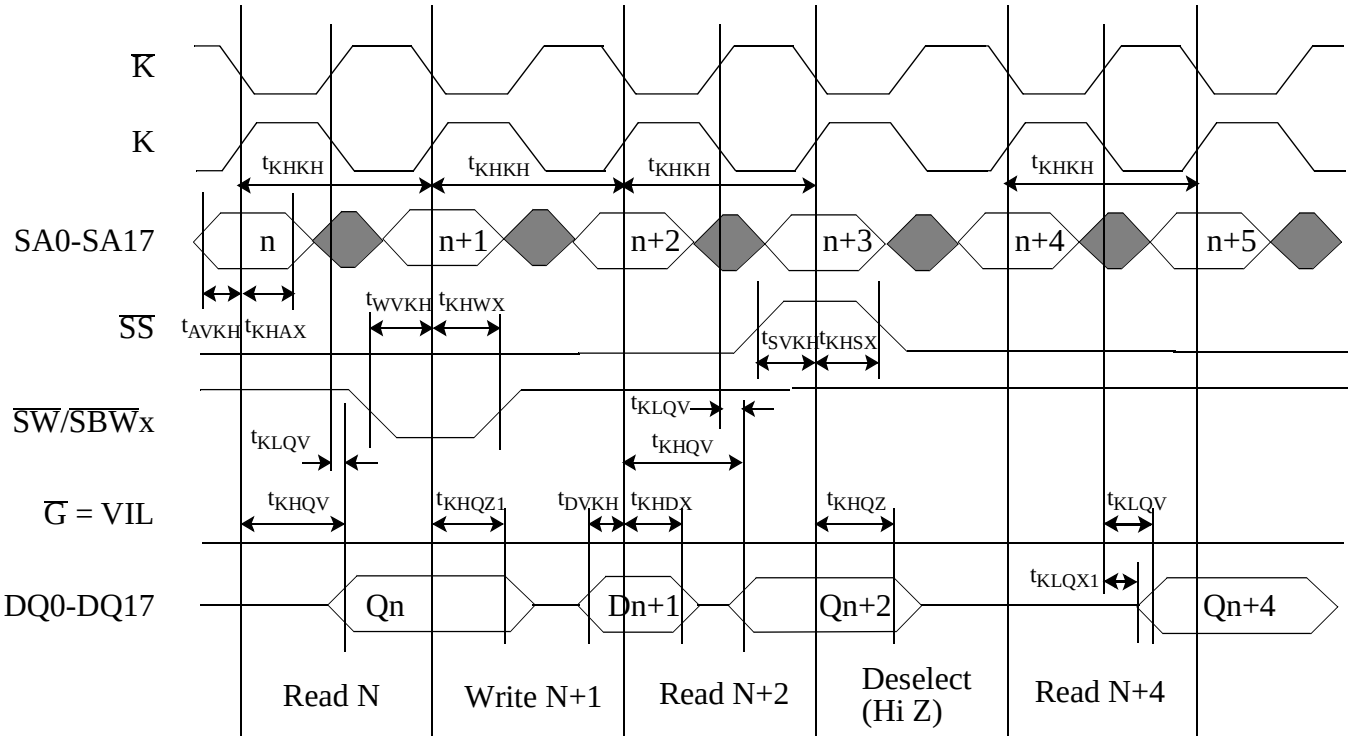



### TIMING WAVEFORM OF WRITE CYCLE



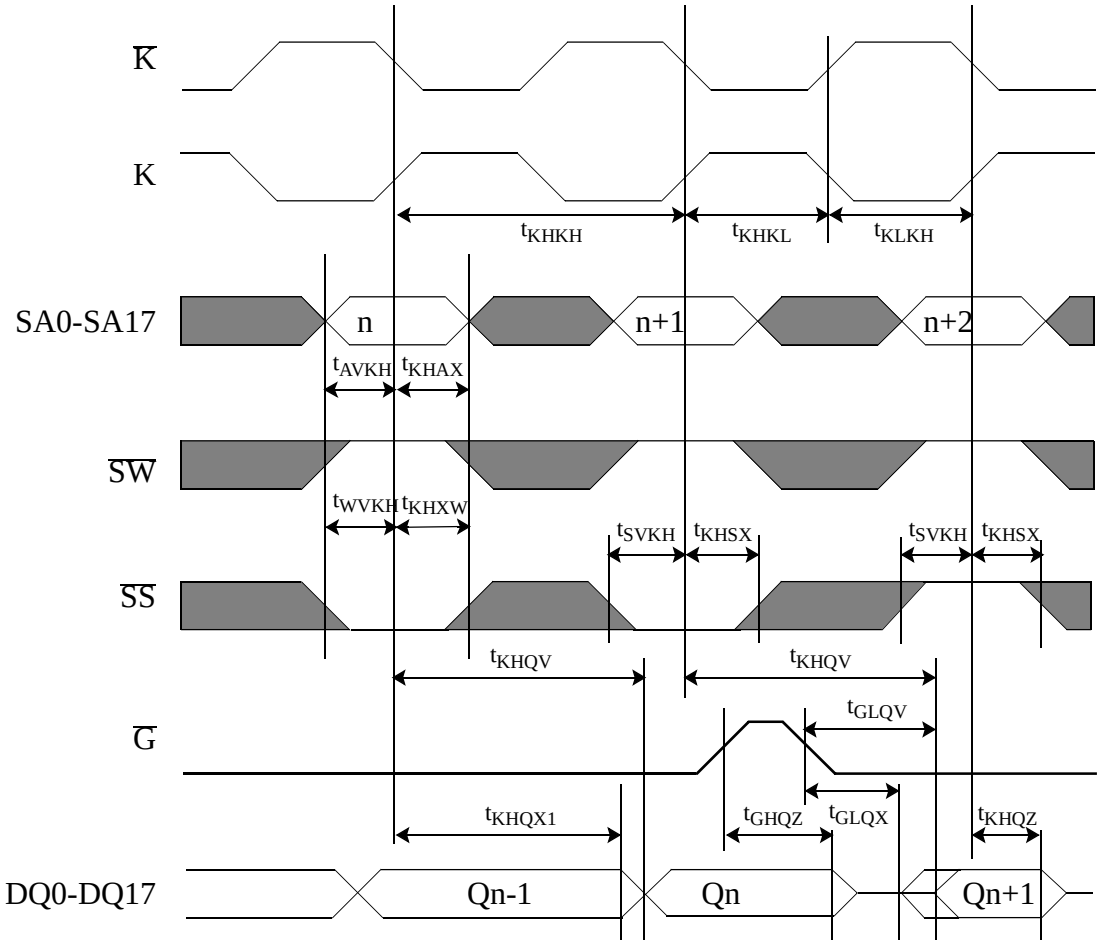
# Register - Latch Mode

## TIMING WAVEFORM OF READ-WRITE-READ CYCLE

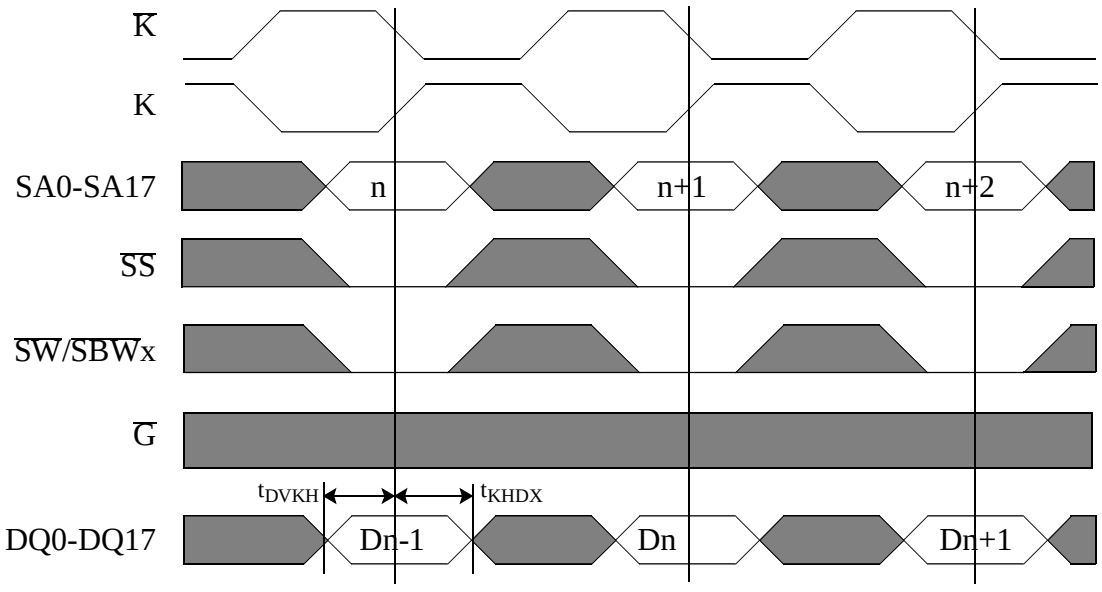


# Register - Flow Thru Mode

## TIMING WAVEFORM OF READ CYCLE

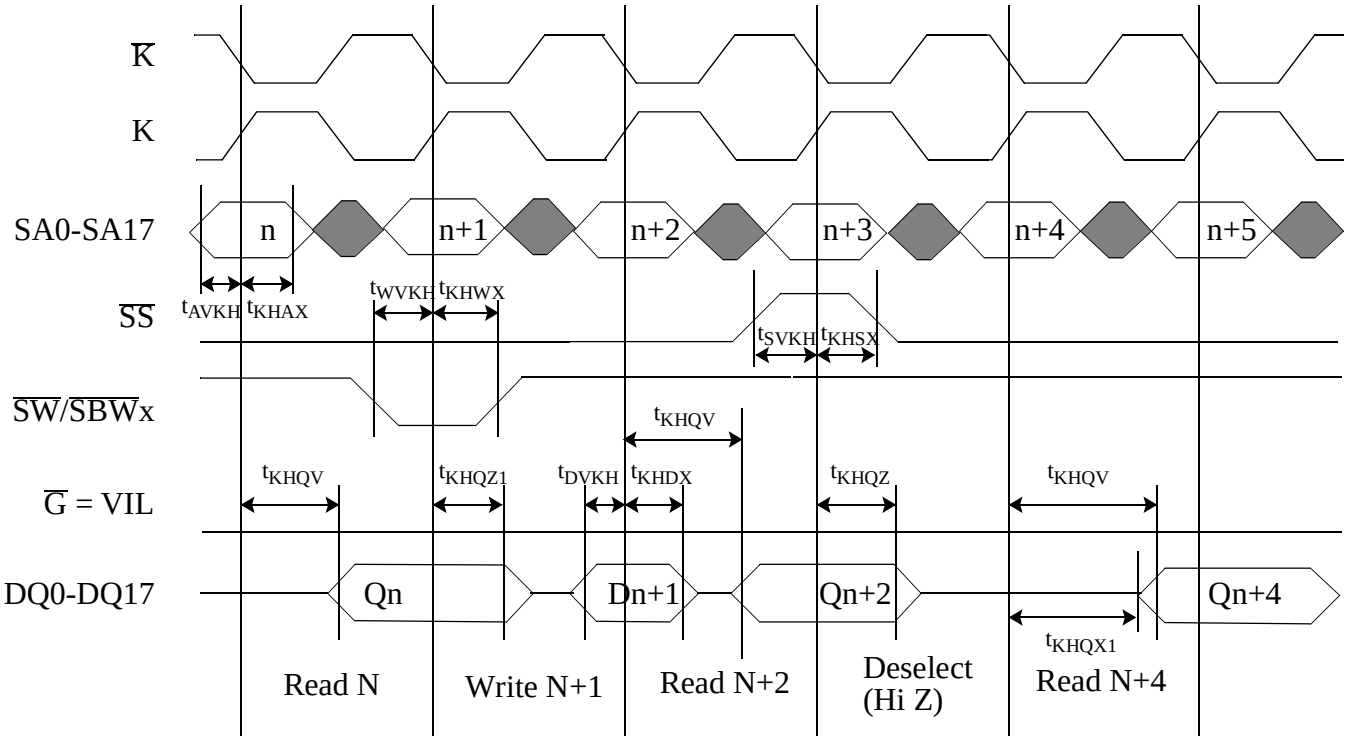



## TIMING WAVEFORM OF WRITE CYCLE



# Register - Flow Thru Mode

## TIMING WAVEFORM OF READ-WRITE-READ CYCLE



# Test Mode Description

## Functional Description

The CXK77B1841 provides a JTAG boundary scan interface using a limited set of IEEE std. 1149.1 functions. The test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), SRAMs, other components and the printed circuit board.

In conformance with a subset of IEEE std. 1149.1, the CXK77B1841 contains a TAP controller, Instruction register, Boundary scan register and Bypass register.

JTAG Inputs/Outputs are LVTTL compatible only.

## Test Access Port (TAP)

4 pins as defined in the Pin Description table are used to perform JTAG functions. The TDI input pin is used to scan test data serially into one of three registers (Instruction register, Boundary Scan register and Bypass register). TDO is the output pin used to scan test data serially out. The TDI pin sends the data into LSB of the selected register and the MSB of the selected register feeds the data to TDO. The TMS input pin controls the state transition of 16 state TAP controller as specified in IEEE std. 1149.1. Inputs on TDI and TMS are registered on the rising edge of TCK clock. The output data on TDO is presented on the falling edge of TCK. TDO driver is in active state only when TAP controller is in Shift-IR state or in Shift-DR state.

TCK, TMS, TDI must be tied low when JTAG is not used.

## TAP Controller

16 state controller is implemented as specified in IEEE std. 1149.1.

The controller enters reset state in one of two ways:

1. Power up.

2. Apply a logic 1 on TMS input pin on 5 consecutive TCK rising edges.

## Instruction Register (3 bits)

The JTAG Instruction register consists of a shift register stage and parallel output latch. The register is 3 bits wide and is encoded as follow:

| Octal | MSB.....LSB | | | Instruction |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Bypass |
| 1 | 0 | 0 | 1 | IDCODE. Read device ID |
| 2 | 0 | 1 | 0 | Sample-Z. Sample Inputs and tri-state DQs |
| 3 | 0 | 1 | 1 | Bypass |
| 4 | 1 | 0 | 0 | Sample. Sample Inputs. |
| 5 | 1 | 0 | 1 | Private. Manufacturer use only. |
| 6 | 1 | 1 | 0 | Bypass |
| 7 | 1 | 1 | 1 | Bypass |

**Bypass Register (1 bit)**

The Bypass Register is one bit wide and is connected electrically between TDI and TDO and provides the minimum length serial path between TDI and TDO.

**ID Registers (32 bits)**

The ID Register is 32 bits wide and is encoded as follows:

| | ID[0} | 1 |
|---|---|---|
| Sony ID | ID[11:1] | 0000 1110 001 |
| Part Number | ID[27:12] | 0000 0000 0001 1010 |
| Revision Number | ID[31:28] | xxxx |

**Boundary Scan Register (51 bits)**

The Boundary Scan Registers are 51 bits wide and are listed as follows:

| | |
|---|---|
| DQ | 18 |
| SA | 18 |
| $\overline{SW}$, $\overline{SBW}$x | 3 |
| $\overline{SS}$, $\overline{G}$ | 2 |
| K, $\overline{K}$, C, $\overline{C}$ | 4 |
| ZZ | 1 |
| M1, M2 | 2 |
| Place Holder | 2 |
| TNC | 1 |

K/$\overline{K}$, C/$\overline{C}$ inputs are sampled through one differential stage and internally inverted to generate internal K/$\overline{K}$, C/$\overline{C}$ signals for scan registers. Place Holder are required for some NC pins to maintain 51 bits Scan Register for different types of the same family SRAM and for density upgrades. All Place Holder Registers are connected to $V_{SS}$ internally regardless of pin connection externally. TNC register is True No Connect i.e. not connected internally. TNC register information should be ignored during BSCAN testing.

**Scan Order (Order by exit sequence)**

| | | | | | | |
|---|---|---|---|---|---|---|
| 26 | 3B | SA | | SA | 5B | 25 |
| 27 | - | $V_{SS}$ | | $V_{SS}$ | - | 24 |
| 28 | 3A | SA | | SA | 5A | 23 |
| 29 | 3C | SA | | SA | 5C | 22 |
| 30 | 2C | SA | | SA | 6C | 21 |
| 31 | 2A | SA | | SA | 6A | 20 |
| 32 | 1D | DQb | | DQa | 6D | 19 |
| 33 | 2E | DQb | | DQa | 7E | 18 |
| 34 | 2G | DQb | | DQa | 6F | 17 |
| 35 | 1H | DQb | | DQa | 7G | 16 |
| 36 | 3G | $\overline{\text{SBW}}$b | | DQa | 6H | 15 |
| 37 | 4D | TNC(*) | | $\overline{\text{G}}$ | 4F | 14 |
| 38 | 4E | $\overline{\text{SS}}$ | | K | 4K | 13 |
| 39 | 4G | $\overline{\text{C}}$ | | $\overline{\text{K}}$ | 4L | 12 |
| 40 | 4H | C | | $\overline{\text{SBW}}$a | 5L | 11 |
| 41 | 4M | $\overline{\text{SW}}$ | | DQa | 7K | 10 |
| 42 | 2K | DQb | | DQa | 6L | 9 |
| 43 | 1L | DQb | | DQa | 6N | 8 |
| 44 | 2M | DQb | | DQa | 7P | 7 |
| 45 | 1N | DQb | | ZZ | 7T | 6 |
| 46 | 2P | DQb | | SA | 5T | 5 |
| 47 | 3T | SA | | SA | 6R | 4 |
| 48 | 2R | SA | | SA | 4P | 3 |
| 49 | 4N | SA | | SA | 6T | 2 |
| 50 | 2T | SA | | M2 | 5R | 1 |
| 51 | 3R | M1 | | | | |

(*) TNC means that the voltage polarity of this bit should be ignored during boundary scan testing.

## Ordering Information.

| Part Number | Speed | |
|---|---|---|
| | Register - Register | Register - Latch/ Register - Flow Thru |
| CXK77B1841GB-45 | 4.5ns Cycle / 2.4ns Access | 5.5ns Cycle / 5.5ns Access |
| CXK77B1841GB-5 (*) | 5.0ns Cycle / 2.5ns Access | 5.7ns Cycle / 5.7ns Access |
| CXK77B1841GB-6 | 6.0ns Cycle / 3.0ns Access | 6.0ns Cycle / 6.0ns Access |

Note (*): Contact Sony Memory Marketing for availability of “-5” speed bin.

## Revision History

| Rev. # | Rev. date | Changes / Modifications to Data-Sheet |
|---|---|---|
| rev 4.0 | 8/22/97 | Initial version, based on TS-2 evaluation |
| rev 4.2 (Unreleased) | 11/21/97 | Modified AC Electrical Characteristics:<br>R-L, R-FT Modes:<br>-6 $T_{KLQV}$, $T_{GLQV,}$ $T_{GHQZ}$ 3.0ns to 2.5ns<br>$T_{KHQZ}$, $T_{KHQZ1}$ 3.0ns to 2.0ns<br>$T_{KHQX1}$ 2.0ns to 3.0ns<br><br>Renamed “-4.5” bin to “-45” bin in all modes.<br>Renamed “-5” bin to “-50” bin in all modes.<br>Renamed “-6” bin to “-60” bin in all modes.<br>Added “-65” bin to all modes.<br><br>Provided IDD & ISB typical values (page-7)<br>Provided PECL DC electrical characteristic (page-6)<br>Provided PECL AC test conditions (page-10, -11) |
| rev 4.3 | 01/05/98 | Updated DC Recommended Operating Conditions (page-6)<br>Updated AC Test Conditions for $V_{DDQ}$ = 2.5V (page-10) |
| rev 4.4 | 01/15/98 | Deleted “-65” bins. |
| rev 4.5 | 03/12/98 | Renamed “-50” bin to “-5” bin in all modes.<br>Renamed “-60” bin to “-6” bin in all modes.<br><br>Changed BSCAN register # 37 from $V_{SS}$ to TNC (page-20)<br>Modified BSCAN register table to include TNC (page-19)<br><br>$T_{KHQZ}$ & $T_{KHQZ1}$ AC timing changed to 2.0ns for all bins (page-8 &-9)<br><br>Changed $V_{DIF}$ (min) DC parameter from 0.4V to 0.5V (page-6)<br>Changed $V_{CM}$ (min) DC parameter from 1.2V to 1.15V (page-6)<br>Changed $V_{CM}$ (typ) DC parameter from $V_{DDQ}$/2 to 1.4V (page-6)<br>Deleted LVTTL Clock $V_{IH}$ and $V_{IL}$ DC parameters (page-6)<br>Added LVTTL Clock $V_{KIN}$ DC parameter (page-6)<br>Added LVTTL Clock $V_X$ DC parameter (page-6)<br>Added Note 5 (Clock description) to DC Recommendations (page-6)<br><br>Rearranged AC Test Conditions (page-10 & page-11)<br>Removed “Preliminary” from the spec. |
| rev 4.6 | 08/12/98 | Modified AC Electrical Characteristics:<br>R-R Mode:<br>-45 $T_{KHQV}$ 2.3ns to 2.4ns |