SONY

Ultra-High Linearity SPDT Switch

CXM3592AUR

Description

The CXM3592AUR is a high power and ultra-high linearity SPDT switch for wireless communication systems.
The CXM3592AUR can be used for SVLTE and carrier aggregation requiring very high linearity.
This IC has a 1.8 V CMOS compatible decoder.
The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and ultra-high linearity.
(Application: LTE/CDMA/GSM/UMTS Handsets and mini base-stations)

Features

- ◆Insertion loss: 0.22 dB (Typ.) (Cellular Band / GSM Low Band)
  0.43 dB (Typ.) (IMT2000 / GSM High Band)
- ◆Ultra-high linearity: IMD3 = –104 dBm (Max.), IIP3 = 82 dBm (Min.)
  at LTE Band 13, PTx = +23 dBm, PBlocker = +14 dBm
- ◆Low voltage operation: V_{DD} = 2.5 V
- ◆No DC blocking capacitors required on RF ports
- ◆1 control input
- ◆Small package size: UQFN-12 pin (2.0 mm × 2.0 mm)
- ◆Lead-Free and RoHS compliant

Structure

GaAs JPHEMT MMIC switch, CMOS decoder

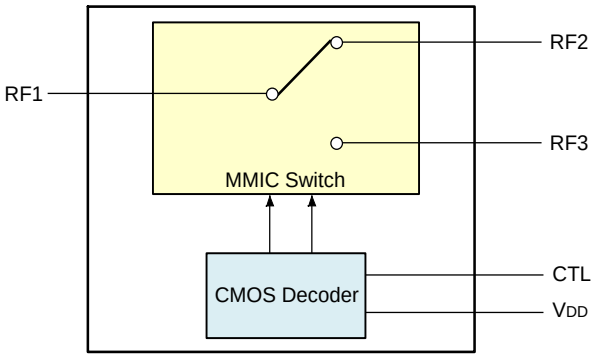
Absolute Maximum Ratings

♦ Bias voltage	V_{DD}	4	V	(Ta = 25 ˚C)
♦ Control voltage	Vctl	4	V	(Ta = 25 ˚C)
♦ Maximum input power		36	dBm	(Duty cycle = 12.5 to 50 %, Ta = 25 ˚C)
♦ Operating temperature	Topr	–35 to +90	˚C	
♦ Storage temperature	Tstg	–65 to +150	˚C	

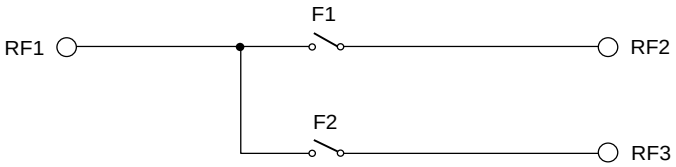
This IC is ESD sensitive device. Special handling precautions are required.

Block Diagram

SPDT Antenna Switch



MMIC Switch

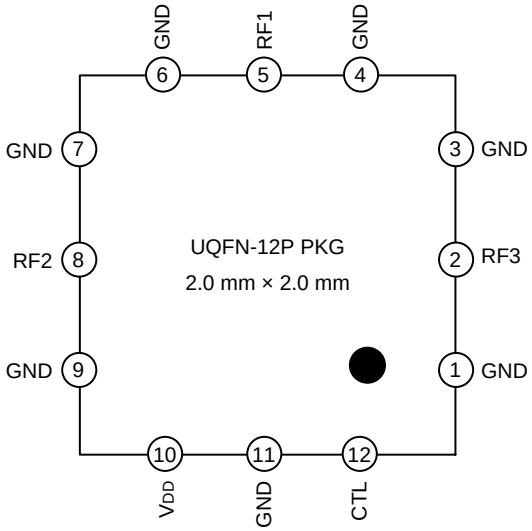


Truth Table

CTL	Active path	F1	F2
L	RF1-RF2	ON	OFF
H	RF1-RF3	OFF	ON

Pin Configuration

(Top View)



DC Bias Condition

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	2.5	2.7	3.3	V
Vctl (H)	1.35	1.8	3.3	
Vctl (L)	0	—	0.45	

Electrical Characteristics

(Ta = 25 °C, V_{DD} = 2.5 V, Vctl = 0/1.8 V)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	RF1-RF2	*1, *2, *6, *8	—	0.22	0.37	dB
			*3, *4, *7, *9	—	0.43	0.58	
			*5	—	0.57	0.77	
		RF1-RF3	*1, *2, *6, *8	—	0.22	0.37	
			*3, *4, *7, *9	—	0.43	0.58	
			*5	—	0.57	0.77	
Isolation	ISO.	RF1-RF2	*1, *2, *6, *8	18	21	—	dB
			*3, *4, *7, *9	11	14	—	
			*5	9	12	—	
		RF1-RF3	*1, *2, *6, *8	18	21	—	
			*3, *4, *7, *9	11	14	—	
			*5	9	12	—	
VSWR	VSWR	All ports in active paths	700 to 2700 MHz	—	—	1.5	—
Harmonics	2fo	RF1-RF2, RF3	*6	—	–60	–41	dBm
	3fo			—	–68	–41	
	2fo		*7	—	–66	–45	
	3fo			—	–72	–45	
	2fo		*2, *3, *5	—	–80	–50	
	3fo			—	–90	–50	
	2fo		*1	—	–82	–78	
Inter modulation distortion in Rx Band	IMD2	RF1-RF2, RF3	*10, *11, *12, *15, *16, *19, *20, *23, *24	—	—	–110	dBm
	IMD3		*10, *13, *14, *17, *18, *21, *22, *25, *26	—	—	–110	
			*10, *27	—	—	–104	dBm
			*10, *28	—	—	–110	dBm
Switching speed	Ts		50 % Ctl to 90 % RF	—	9	13	µs
Wakeup time	Twu		V_{DD} = 2.5 V to 90 % RF, Pin = 0 dBm	—	9	20	µs
Control current	Ictl		Vctl = 1.8 V	—	1	5	µA
Supply current	Idd		V_{DD} = 2.7 V	—	0.14	0.35	mA

Electrical characteristics are measured with all RF ports terminated in 50 Ω.

*1 Pin = 25 dBm, 704 to 787 MHz (Band 13, Band 17)
*2 Pin = 26 dBm, 824 to 960 MHz (Band 5, Band 8)
*3 Pin = 26 dBm, 1710 to 1990 MHz (Band 1 Tx, Band 2 Tx, Band 3 Tx, Band 4 Tx)
*4 Pin = 10 dBm, 2110 to 2170 MHz (Band 1 Rx, Band 4 Rx)
*5 Pin = 26 dBm, 2500 to 2690 MHz (Band 7)
*6 Pin = 35 dBm, 824 to 915 MHz (GSM850/900 Tx)
*7 Pin = 32 dBm, 1710 to 1910 MHz (GSM1800/1900 Tx)
*8 Pin = 10 dBm, 869 to 960 MHz (GSM850/900 Rx)
*9 Pin = 10 dBm, 1805 to 1990 MHz (GSM1800/1900 Rx)
*10 Measured with the recommended circuit.

IMD Condition (1)

Band	fRx on RF [MHz]	fTx +20 dBm on RF [MHz]	fBlocker –15 dBm on RF1 [MHz]		IMD condition
Band 1	2140	1950	IMD2 (fRx – fTx)	190	*11
			IMD2 (fRx + fTx)	4090	*12
			IMD3 (2fTx – fRx)	1760	*13
			IMD3 (2fTx + fRx)	6040	*14
Band 2	1960	1880	IMD2 (fRx – fTx)	80	*15
			IMD2 (fRx + fTx)	3840	*16
			IMD3 (2fTx – fRx)	1800	*17
			IMD3 (2fTx + fRx)	5720	*18
Band 5	880	835	IMD2 (fRx – fTx)	45	*19
			IMD2 (fRx + fTx)	1715	*20
			IMD3 (2fTx – fRx)	790	*21
			IMD3 (2fTx + fRx)	2550	*22
Band 7	2655	2535	IMD2 (fRx – fTx)	120	*23
			IMD2 (fRx + fTx)	5190	*24
			IMD3 (2fTx – fRx)	2415	*25
			IMD3 (2fTx + fRx)	7725	*26

IMD Condition (2)

Band	fRx on RF [MHz]	fTx PTx = +23 dBm on RF [MHz]	fBlocker PBlocker = +14 dBm on RF1 [MHz]		IMD condition
Band 13	747	786	IMD3 (2fTx – fRx)	825	*27
BC0	872	782	IMD3 (fTx + fRx)/2	827	*28

Triple Beat Ratio

(V_{DD} = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition					Min.	Typ.	Max.	Unit
			Input power at RF [dBm]	Tx1 at RF* [MHz]	Tx2 at RF* [MHz]	Jammer at RF1 –30 dBm [MHz]	Triple beat product at RF* [MHz]				
Triple beat ratio	TBR	RF1 - RF2, RF3	21.5	835.5	836.5	881.5	881.5 ± 1	88	—	—	dBc
			21.5	1880	1881	1960	1960 ± 1	88	—	—	
			13.5	1732	1733	2132	2132 ± 1	88	—	—	

* Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit.

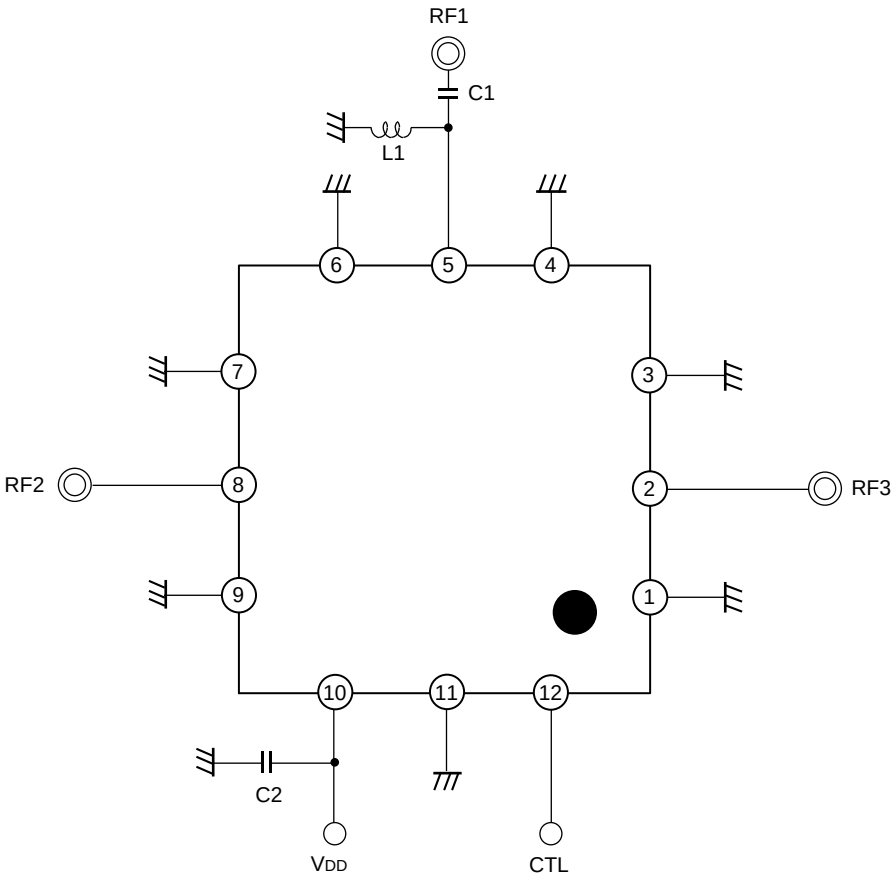
IIP2

(V_{DD} = 2.5 V, Ta = 25 °C)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			Tx at RF* 24 dBm [MHz]	Jammer at RF1 –20 dBm [MHz]	IM2 product at RF* [MHz]				
Input IP2	IIP2	RF1 - RF2, RF3	836.61	1718.61	881.61	113.5	—	—	dBm
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

* Electrical characteristics are measured with all RF ports terminated in 50 Ω.
Measured with the recommended circuit.

Recommended Circuit



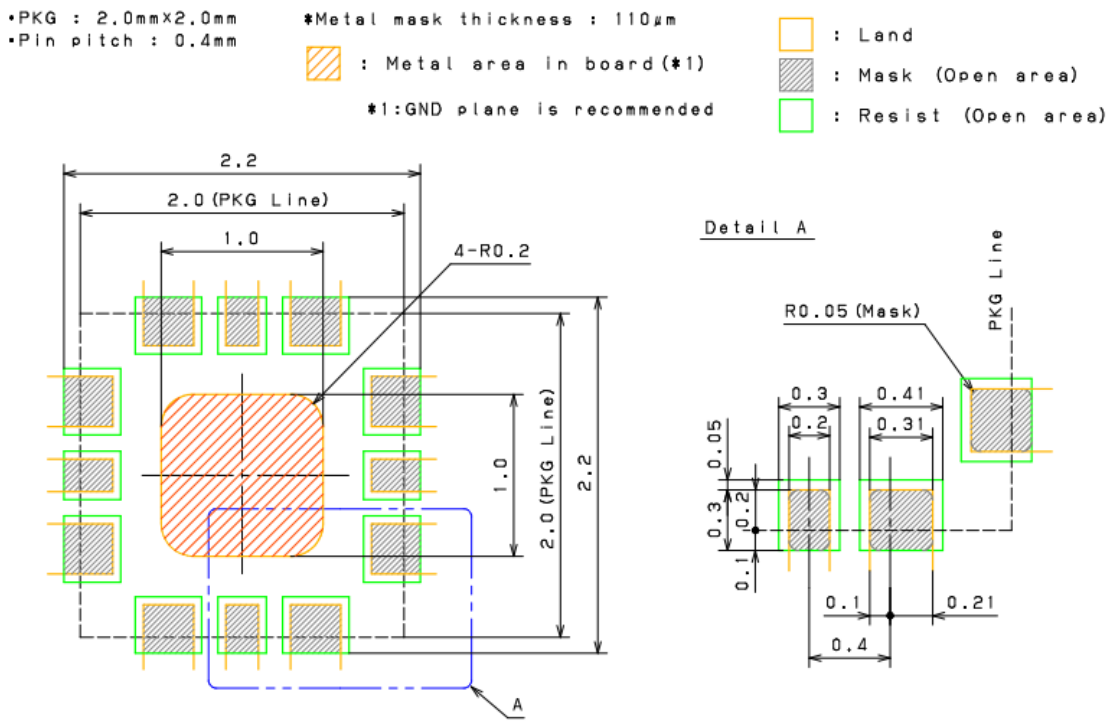
∗1 No DC blocking capacitors are required on all RF ports. (Except sourcing DC bias)

∗2 The DC levels of all RF ports are GND.

∗3 L1 (27 nH) and C1 (12 pF) are recommended on RF1 port for ESD protection.

∗4 C2 (100 pF) is recommended on V_{DD} pin for Decoupling Capacitor.

Recommended Land Pattern

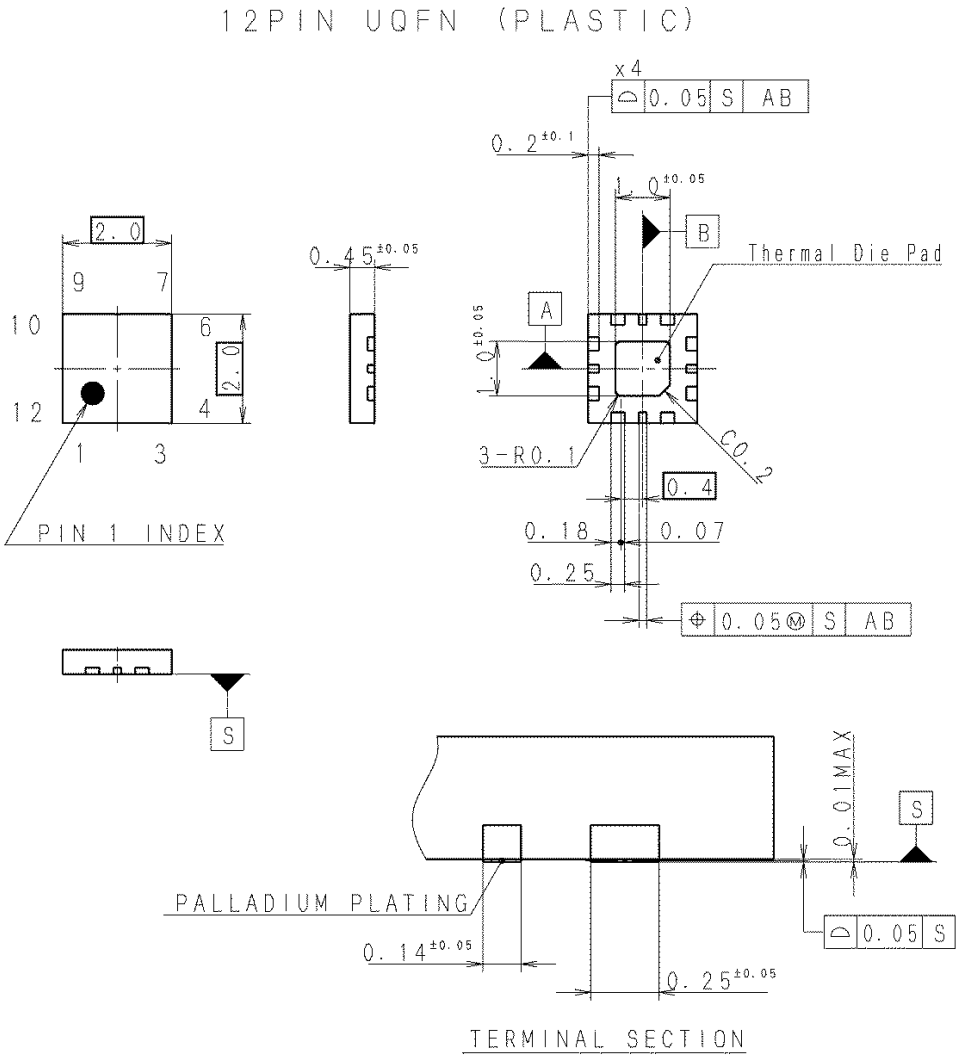


SONY

Package Outline

Product Code : 875340755

(Unit: mm)



Note:Terminal burr height 0.05mm MAX.

SONY CODE	UQFN-12P-053
JEITA CODE	----------
JEDEC CODE	----------

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.006g

PART No. AP-2000-12QND3	Rev. 0
ISSUED '11.11.23	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-12-AD	

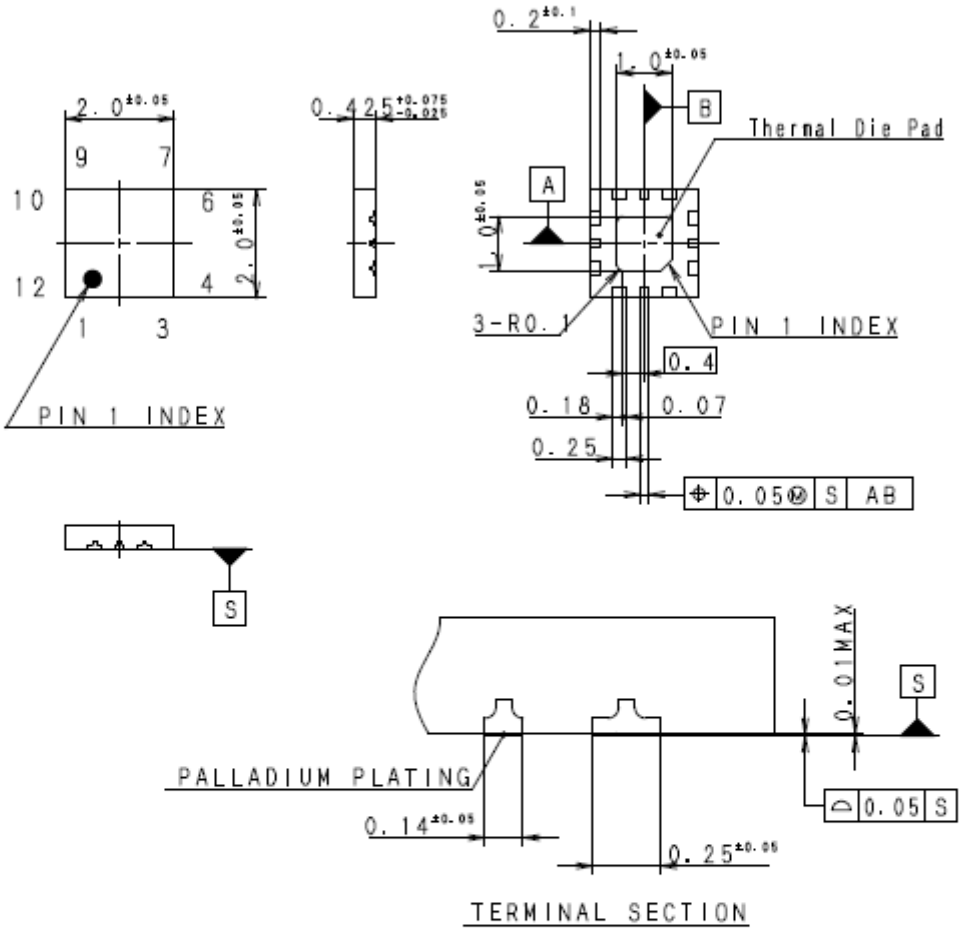
SONY

Package Outline

Product Code : 875342695

(Unit: mm)

12PIN UQFN (PLASTIC)



TERMINAL SECTION

Note:Terminal burr height 0.05mm MAX.

SONY CODE	UQFN-12P-04
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

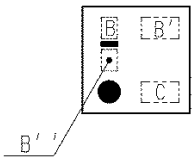
PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.006g

PART No. AP-4000-12016S	Rev. 0
ISSUED '12.09.07	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR
REMARKS PKG CODE:UR-12-A	

SONY

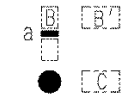
Marking

Product Code : 875340755



MARKING C: GM

注1） B部，B'部，B''部はロット番号（Max4文字）を配置する。
（B部，B'部は通し記号，B''は製造年を配置する。）
注2） C部は製品名（Max2文字）を配置する。
（2文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは，Max0．05mmの事。
注4） a部は組立場所表記を配置する。



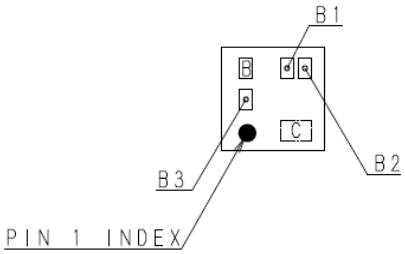
DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 4 CHARACTERS) IN SECTION B, B', B''.
(B, B' :SERIAL CODE, B'' :YEAR OF MANUFACTURE.
2) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm.
4) ASSEMBLY PLACE IN SECTION a.

SONY

Marking

Product Code : 875342695



MARKING C: GM

注1) B, B1, B2部はロット番号（Max3文字通し記号）を配置する。
（B部通し記号3桁の100の位, B1部10の位, B2部1の位を配置する。）
B3部は年コードを配置する。
（規定文字数未満につき省略は省略規定に従う。）
注2) C部は製品名（Max2文字）を配置する。
（2文字を超える場合は製品名省略標示規定に従う。）
注3) マーク深さは, Max0.04mmの事。

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS) IN SECTION B, B1, B2.
(B:HUNDREDS DIGIT, B1:TEN DISIT, B2:ONES DISIT.)
A YEAR CODE IN SECTION B3
(FOLLOW RULES FOR ABBREVIATIONS.)
2) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.04 mm.

SONY

Tape and Reel Size

CXM3592AUR-T9

Product Code：875340755

8mm WIDTH EMBOSSED TAPING

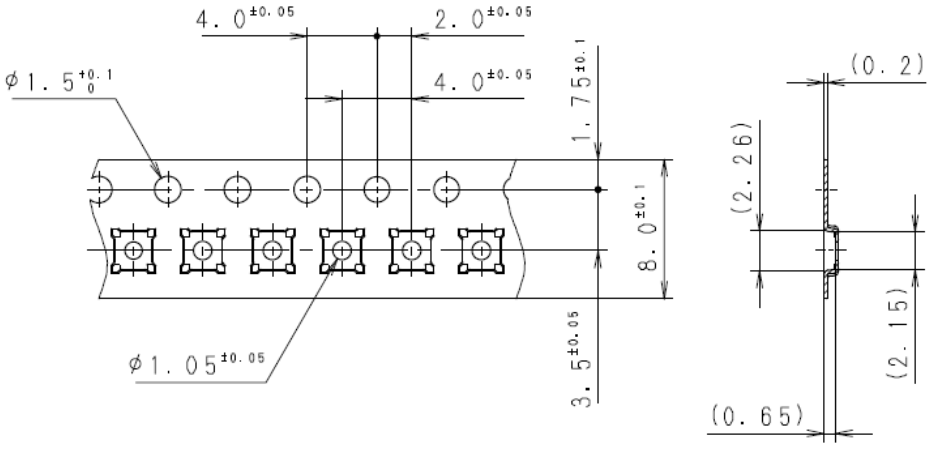
PACKAGE CODE	EMBOSSED TAPING CODE
UQFN-12P-053	R012XN02-08-N-1

1. SCOPE

THIS SPECIFICATION DESCRIBES THE EMBOSSED TAPING FOR SMD(SURFACE MOUNTED DEVICE) IC'S. FOR SHIPMENT. THIS SPECIFICATION IS BASED ON THE STIPULATIONS OF JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION(JEITA). JIS C0806-3. AND ELECTRONIC INDUSTRIES ASSOCIATION EIA-481.

2. PRODUCT INDICATION

3. TAPING SPECIFICATIONS

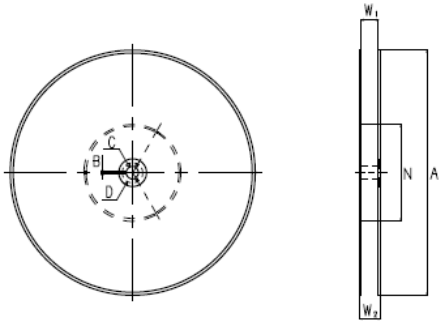


NOTE)1. THE R MEASUREMENT WITHOUT INDICATION IS ASSUMED TO BE 0.3mm MAX. GENERAL TOLERANCE: ±0.2

2. THE FEED HOLE CUMULATIVE PITCH ERROR IS ASSUMED AT±0.2mm/10PITCH. UNIT:mm

4. REEL DIMENSIONS

φ254mm PLASTIC REEL



UNIT:mm

SYMBOL	A	N	C	D
DIMENSION	φ254±2	φ100+4 0	φ13±0.2	φ21±0.8
SYMBOL	B	W_1	W_2	
DIMENSION	2±0.5	9.5±1.0	13.5±1.0	

MATERIAL:POLYSTYRENE CONTAINING CARBON(ANTISTATIC)

*INTRODUCTION OF REUSE REEL
(REEL THAT IS USED AGAIN AFTER COLLECTION)
WE USE THE REUSE REEL OF JEITA SPECIFICATION.

SONY

Tape and Reel Size

CXM3592AUR-T9

Product Code：875342695

8mm WIDTH EMBOSSED TAPING

PACKAGE CODE	EMBOSSED TAPING CODE
UQFN-12P-04	R012UN26-08-N-2

1. SCOPE

THIS SPECIFICATION DESCRIBES THE EMBOSSED TAPING FOR SMD(SURFACE MOUNTED DEVICE) IC'S. FOR SHIPMENT. THIS SPECIFICATION IS BASED ON THE STIPULATIONS OF JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION(JEITA), JIS C0806-3, AND ELECTRONIC INDUSTRIES ASSOCIATION EIA-481.

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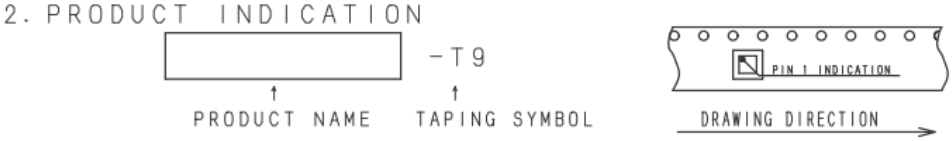

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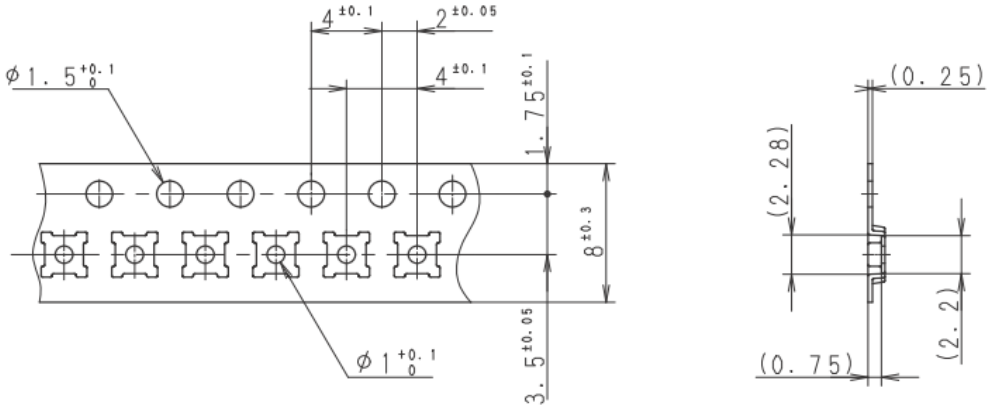
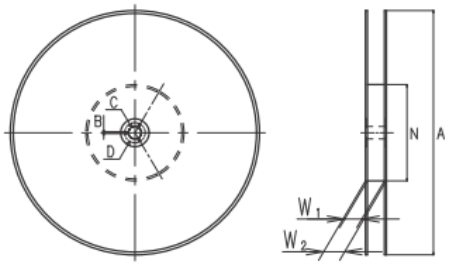


NOTE)1. THE R MEASUREMENT WITHOUT INDICATION IS ASSUMED TO BE 0.3mm MAX.
2. THE FEED HOLE CUMULATIVE PITCH ERROR IS ASSUMED AT±0.2mm/10PITCH.

GENERAL TOLERANCE: ±0.2
UNIT: mm

4. REEL DIMENSIONS

φ254mm PLASTIC REEL



UNIT: mm

SYMBOL	A	N	C	D
DIMENSION	φ254±2	φ100 +2 0	φ13±0.2	φ21±0.8
SYMBOL	B	W_1	W_2	
DIMENSION	2±0.5	9.4±1.0	13.4±1.0	

MATERIAL: POLYSTYRENE CONTAINING CARBON(ANTISTATIC)

*INTRODUCTION OF REUSE REEL
(REEL THAT IS USED AGAIN AFTER COLLECTION)
WE USE THE REUSE REEL OF JEITA SPECIFICATION.

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Note

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