

POWER SAVING SOLENOID CONTROLLER WITH INTEGRATED SUPPLY REGULATION

Check for Samples: [DRV110](#)

FEATURES

- Drives an External MOSFET With PWM to Control Solenoid Current
 - External Sense Resistor for Regulating Solenoid Current
- Fast Ramp-Up of Solenoid Current to Guarantee Activation
- Solenoid Current is Reduced in Hold Mode for Lower Power and Thermal Dissipation
- Ramp Peak Current, Keep Time at Peak Current, Hold Current and PWM Clock Frequency Can Be Set Externally. They Can Also Be Operated at Nominal Values Without External Components.
- Internal Supply Voltage Regulation
 - 15-V Nominal MOSFET Gate Drive Voltage
- External Pull-Up Resistor to Solenoid Supply Voltage
- Protection
 - Thermal Shutdown
 - Under Voltage Lockout (UVLO)
 - Maximum Ramp Time
 - Optional STATUS Output
- Operating Temperature Range: -40°C to 105°C
- 8-Pin and 14-Pin TSSOP Package Options

APPLICATIONS

- Electromechanical Driver: Solenoids, Valves, Relays
- White Goods, Solar, Transportation

DESCRIPTION

The DRV110 is a PWM current controller for solenoids. It is designed to regulate the current with a well controlled waveform to reduce power dissipation. The solenoid current is ramped up fast to ensure opening of the valve or relay. After initial ramping the solenoid current is kept at peak value to ensure the correct operation, after which it is reduced to a lower hold level in order to avoid thermal problems and reduce power dissipation.

The peak current duration is set with an external capacitor. The current ramp peak and hold levels, as well as PWM frequency can independently be set with external resistors. External setting resistors can also be omitted, if the default values for the corresponding parameters are suitable for the application.

The DRV110 limits its own supply at VIN to 15 V which is also the gate drive voltage of an external switching device. For example, a MOSFET that is driving the solenoid load. If a lower gate drive voltage is required, an external supply of at least 6 V can be used.

ORDERING INFORMATION⁽¹⁾

PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
(TSSOP-8) - PW	Reel of 2000	DRV110PWR	110
(TSSOP-14) - PW	Reel of 2000	DRV110APWR	110A

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TYPICAL APPLICATION

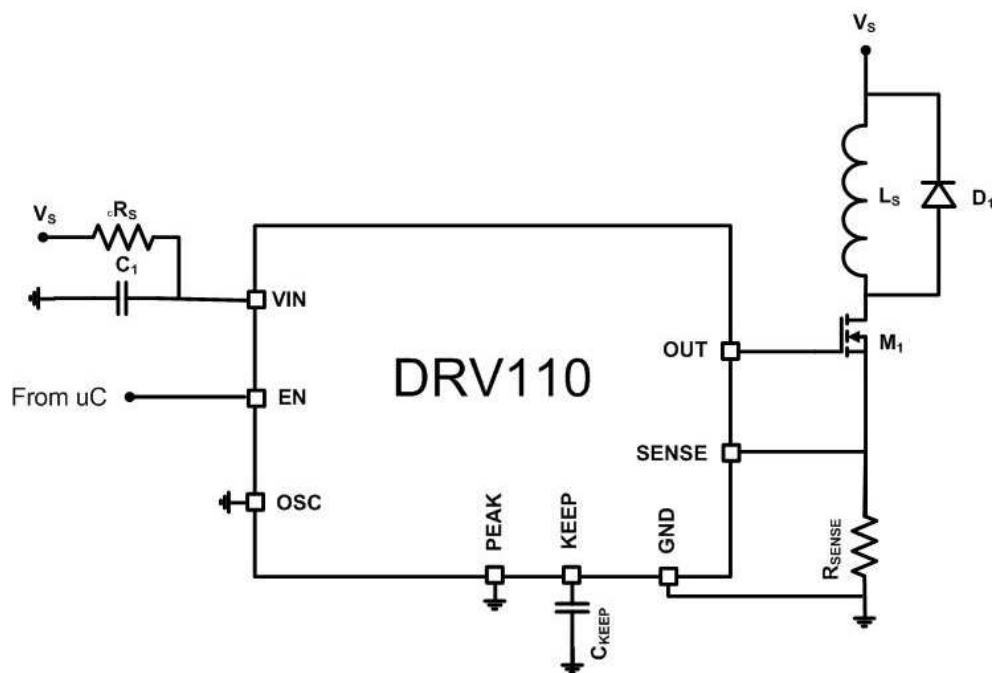


Figure 1. Default Configuration With 8-Pin TSSOP Option

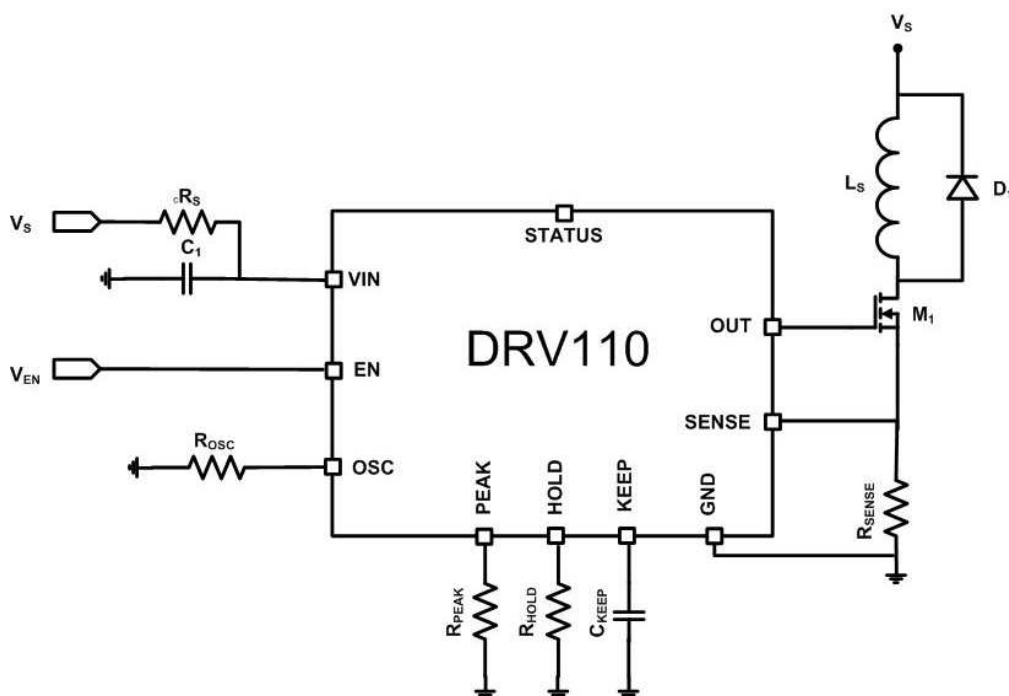


Figure 2. External Parameter Setting for 14-Pin TSSOP Option

DEVICE INFORMATION

Functional Block Diagram

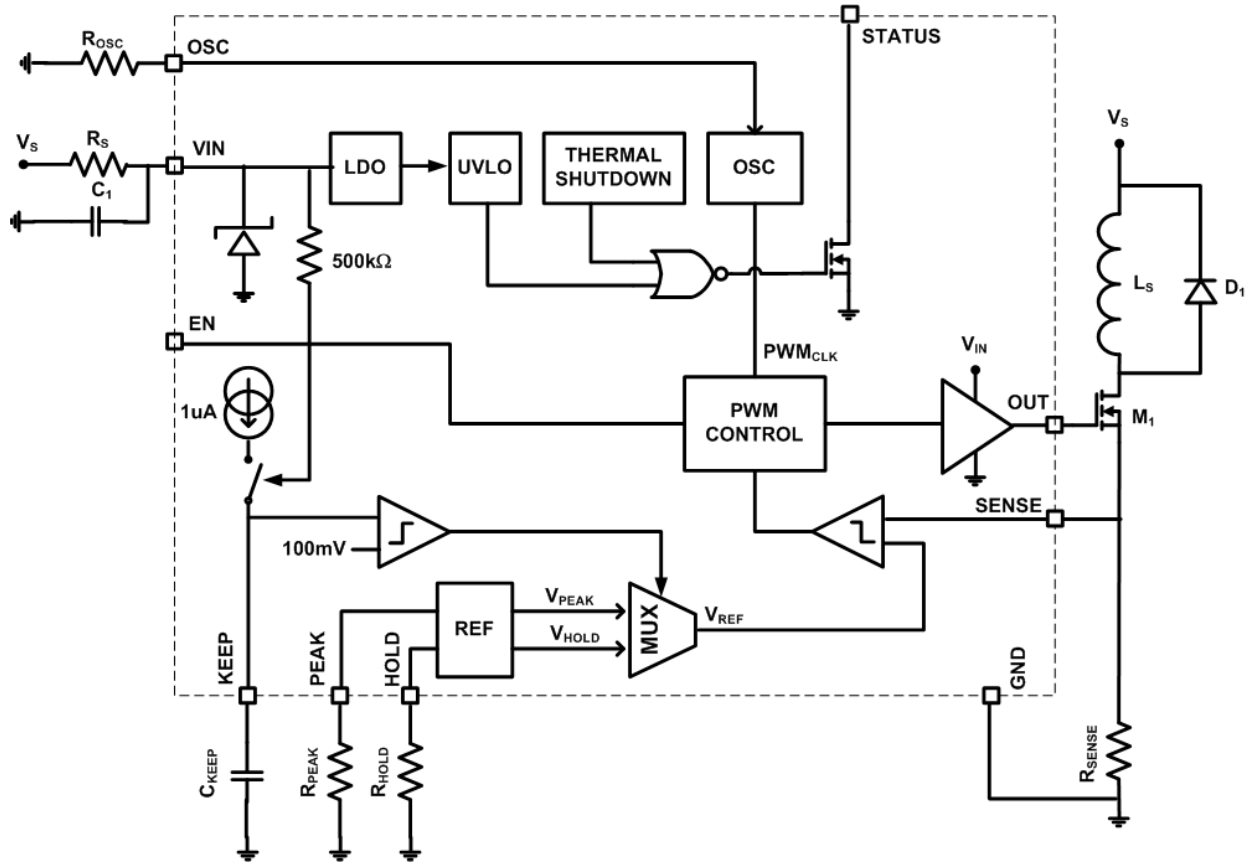
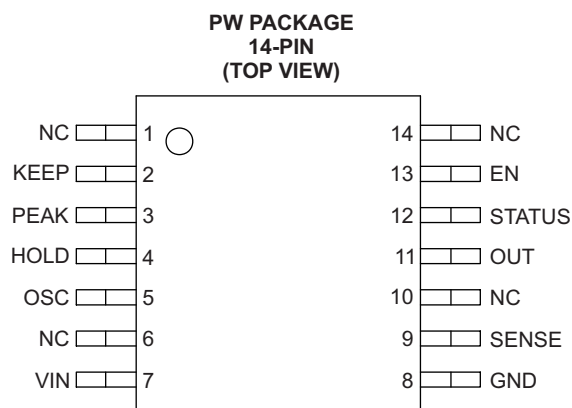
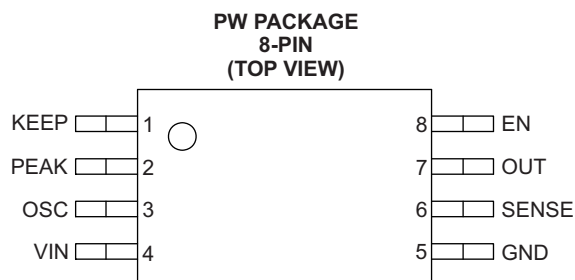


Table 1. TERMINAL FUNCTIONS

NAME	PIN (8-PIN PW) ⁽¹⁾	PIN (14-PIN PW)	DESCRIPTION
KEEP	1	2	Keep time set
PEAK	2	3	Peak current set
HOLD	-	4	Hold current set
OSC	3	5	PWM frequency set
VIN	4	7	6-V to 18-V supply
GND	5	8	Ground
SENSE	6	9	Solenoid current sense
OUT	7	11	Solenoid switch gate drive
STATUS	-	12	Open drain fault indicator
EN	8	13	Enable
NC	-	1, 6, 10, 14	No connect

(1) In the 8-pin package, the HOLD pin is not bonded out. For this package, the HOLD mode is configured to default (internal) settings.



ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

		VALUE	UNIT
V _{IN}	Input voltage range	–0.3 to 20	V
Voltage range on EN, STATUS, PEAK, HOLD, OSC, SENSE, KEEP		–0.3 to 7	V
Voltage range on OUT		–0.3 to 20	V
ESD rating	HBM (human body model)	2000	V
	CDM (charged device model)	500	
T _J	Operating virtual junction temperature range	–40 to 125	°C
T _{stg}	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I _Q	Supply current	1	1.5	3	mA
V _{IN}	Device will start sinking current when V _{IN} > 15 V to limit V _{IN}	6	15		V
C _{IN}	Input capacitor between V _{IN} and GND ⁽¹⁾	1	4.7		μF
L	Solenoid inductance		1		H
T _A	Operating ambient temperature	–40		105	°C

- (1) 4.7-μF input capacitor and full wave rectified 230-Vrms AC supply results in approximately 500-mV supply ripple.

THERMAL INFORMATION

THERMAL METRIC		DRV110		UNITS
		PWP		
		8 PINS	14 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽¹⁾	183.8	122.6	°C/W
θ_{JCTop}	Junction-to-case (top) thermal resistance ⁽²⁾	69.2	51.2	
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	112.6	64.3	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	10.4	6.5	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	110.9	63.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance ⁽⁶⁾	N/A	N/A	

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 14\text{ V}$, $T_A = -40^{\circ}\text{C}$ to 105°C , over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I _Q	Standby current	EN = 0, V _{IN} = 14 V, bypass deactivated		200	250	μA
	Quiescent current	EN = 1, V _{IN} = 14 V, bypass deactivated		360	570	
	Internally regulated supply	EN = 0, I _{VIN} = 2 mA, bypass activated	10.5	15	19	V
		EN = 1, I _{VIN} = 2 mA, bypass activated	14.5	15	15.5	
GATE DRIVER						
V _{DRV}	Gate drive voltage	Supply voltage in regulation (I _{VIN} > 1 mA)		V _{IN}		V
I _{DRV_SINK}	Gate drive sink current	V _{OUT} = 15 V; V _{IN} = 15 V	8	15		mA
I _{DRV_SOURCE}	Gate drive source current	V _{OUT} = GND; V _{IN} = 15 V		-15	-10	mA
f _{PWM}	PWM clock frequency	OSC = GND	15	20	27	kHz
D _{MAX}	Maximum PWM duty cycle			100		%
D _{MIN}	Minimum PWM duty cycle			7.5		%
t _D	Start-up delay	Delay between EN going high until gate driver starts switching, f _{PWM} = 20 kHz			50	μs
CURRENT CONTROLLER, INTERNAL SETTINGS						
I _{PEAK}	Peak current	R _{SENSE} = 1 Ω, PEAK = GND	270	300	330	mA
I _{HOLD}	Hold current	R _{SENSE} = 1 Ω, HOLD = GND	40	50	65	mA
CURRENT CONTROLLER, EXTERNAL SETTINGS						
t _{KEEP}	Externally set keep time at peak current	C _{KEEP} = 1 μF		100		ms
V _{PEAK}	Externally set V _{PEAK}	R _{PEAK} = 50 kΩ		900		mV
		R _{PEAK} = 200 kΩ		300		
V _{HOLD}	Externally set V _{HOLD}	R _{HOLD} = 50 kΩ		150		mV
		R _{HOLD} = 200 kΩ		50		
f _{PWM}	Externally set PWM clock frequency	R _{OSC} = 50 kΩ		60		kHz
		R _{OSC} = 200 kΩ		20		
LOGIC INPUT LEVELS (EN)						
V _{IL}	Input low level				1.3	V
V _{IH}	Input high level		1.65			V
R _{EN}	Input pull-up resistance		350	500		kΩ
LOGIC OUTPUT LEVELS (STATUS)						
V _{OL}	Output low level	Pull-down activated, I _{STATUS} = 2 mA			0.3	V
I _{IL}	Output leakage current	Pull-down deactivated, V(STATUS) = 5 V			2	μA
UNDERVOLTAGE LOCKOUT						
V _{UVLO}	Undervoltage lockout threshold			4.6		V
THERMAL SHUTDOWN						
T _{TSU}	Junction temperature startup threshold			140		°C
T _{TSD}	Junction temperature shutdown threshold			160		°C

FUNCTIONAL DESCRIPTION

DRV110 controls the current through the solenoid as shown in Figure 3. Activation starts when EN pin voltage is pulled high either by an external driver or internal pull-up. In the beginning of activation, DRV110 allows the load current to ramp up to the peak value I_{PEAK} and it regulates it at the peak value for the time, t_{KEEP} , before reducing it to I_{HOLD} . The load current is regulated at the hold value as long as the EN pin is kept high. The initial current ramp-up time depends on the inductance and resistance of the solenoid. Once EN pin is driven to GND, DRV110 allows the solenoid current to decay to zero.

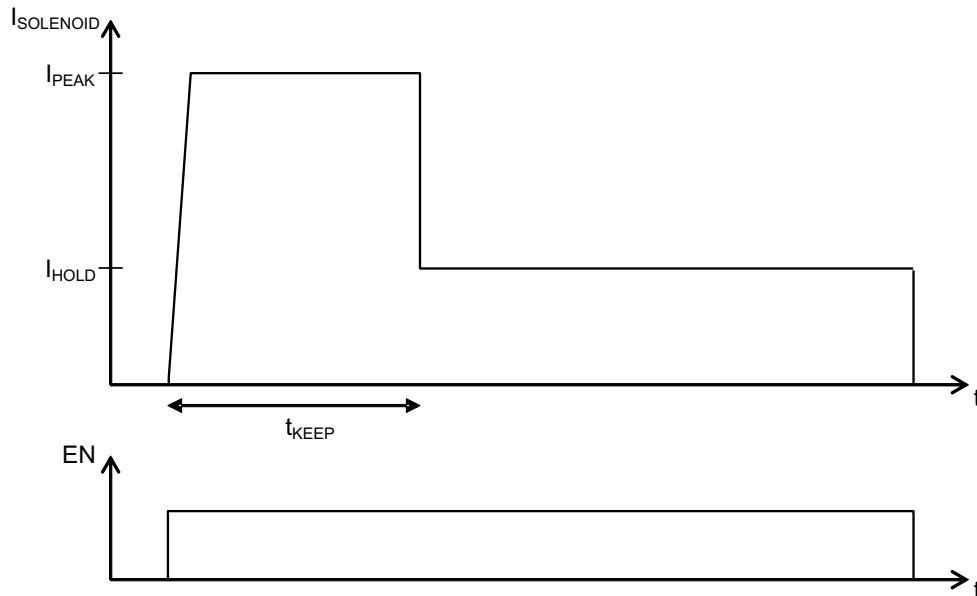


Figure 3. Typical Current Waveform Through the Solenoid

t_{KEEP} is set externally by connecting a capacitor to the KEEP pin. A constant current is sourced from the KEEP pin that is driven into an external capacitor resulting in a linear voltage ramp. When the KEEP pin voltage reaches 100 mV, the current regulation reference voltage, V_{REF} , is switched from V_{PEAK} to V_{HOLD} . Dependency of t_{KEEP} from the external capacitor size can be calculated by:

$$t_{KEEP} [s] = C_{KEEP} [F] \cdot 10^5 \left[\frac{s}{F} \right] \quad (1)$$

The current control loop regulates, cycle-by-cycle, the solenoid current by sensing voltage at the SENSE pin and controlling the external switching device gate through the OUT pin. During the ON-cycle, the OUT pin voltage is driven and kept high (equal to V_{IN} voltage) as long as the voltage at the SENSE pin is less than V_{REF} allowing current to flow through the external switch. As soon as the voltage at the SENSE pin is above V_{REF} , the OUT pin voltage is immediately driven and kept low until the next ON-cycle is triggered by the internal PWM clock signal. In the beginning of each ON-cycle, the OUT pin voltage is driven and kept high for at least the time determined by the minimum PWM signal duty cycle, D_{MIN} .

V_{PEAK} and V_{HOLD} depend on fixed resistance values R_{PEAK} and R_{HOLD} as shown in Figure 4. If the PEAK pin is connected to ground, the peak current reference voltage, V_{PEAK} , is at its default value (internal setting). The V_{PEAK} value can alternatively be set by connecting an external resistor to ground from the PEAK pin. For example, if a 50-k Ω ($= R_{PEAK}$) resistor is connected between PEAK and GND, and $R_{SENSE} = 1 \Omega$, then the externally set I_{PEAK} level will be 900 mA. If $R_{PEAK} = 200 \text{ k}\Omega$ and $R_{SENSE} = 1 \Omega$, then the externally set I_{PEAK} level will be 300 mA. In case $R_{SENSE} = 2 \Omega$ instead of 1 Ω , then $I_{PEAK} = 450 \text{ mA}$ (when $R_{PEAK} = 50 \text{ k}\Omega$) and $I_{PEAK} = 150 \text{ mA}$ (when $R_{PEAK} = 200 \text{ k}\Omega$). External setting of the HOLD current, I_{HOLD} , works in the same way, but the current levels are 1/6 of the I_{PEAK} levels. External settings for I_{PEAK} and I_{HOLD} are independent of each other. If R_{PEAK} is decreased below 33.33 k Ω (typ value), then the reference is clamped to the internal setting. The same is valid for R_{HOLD} and I_{HOLD} . I_{PEAK} and I_{HOLD} values can be calculated by using the formula below.

$$I_{PEAK} = \frac{1\Omega}{R_{SENSE}} \cdot \frac{900\text{mA}}{R_{PEAK}} \cdot 66.67\text{k}\Omega; 66.67\text{k}\Omega < R_{PEAK} < 2\text{M}\Omega \quad (2)$$

$$I_{\text{HOLD}} = \frac{1\Omega}{R_{\text{SENSE}}} \cdot \frac{150\text{mA}}{R_{\text{HOLD}}} \cdot 66.67\text{k}\Omega; 66.67\text{k}\Omega < R_{\text{HOLD}} < 333\text{k}\Omega \quad (3)$$

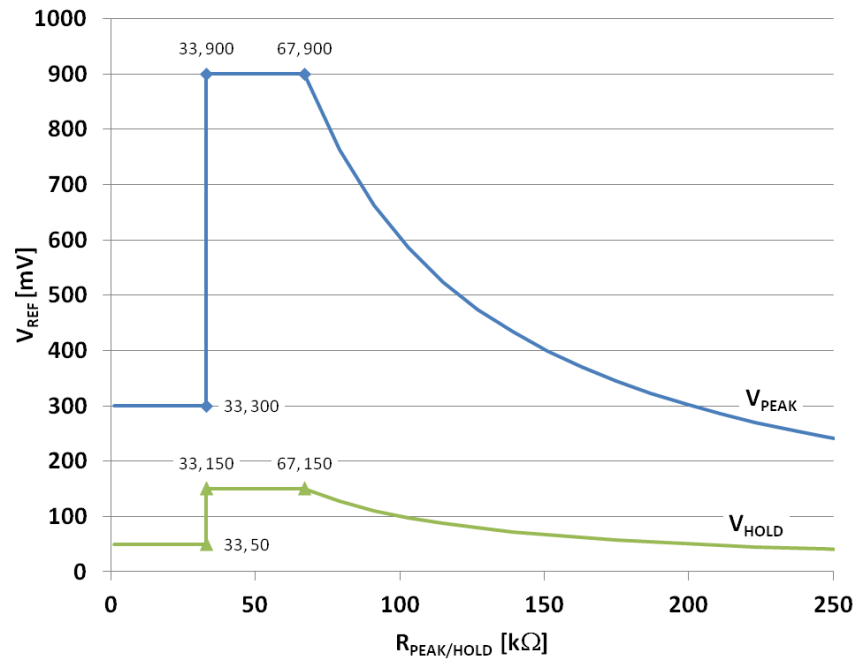


Figure 4. PEAK and HOLD Mode V_{REF} Settings

Frequency of the internal PWM clock signal, PWM_{CLK} , that triggers each OUT pin ON-cycle can be adjusted by external resistor, R_{OSC} , connected between OSC and GND. Frequency as a function of resistor value is shown in Figure 5. Default frequency is used when OSC is connected to GND directly. PWM frequency as a function of external fixed adjustment resistor value (greater than 66.67 k Ω) is given below.

$$f_{PWM} = \frac{60\text{kHz}}{R_{OSC}} \cdot 66.67\text{k}\Omega; 66.67\text{k}\Omega < R_{OSC} < 2\text{M}\Omega \quad (4)$$

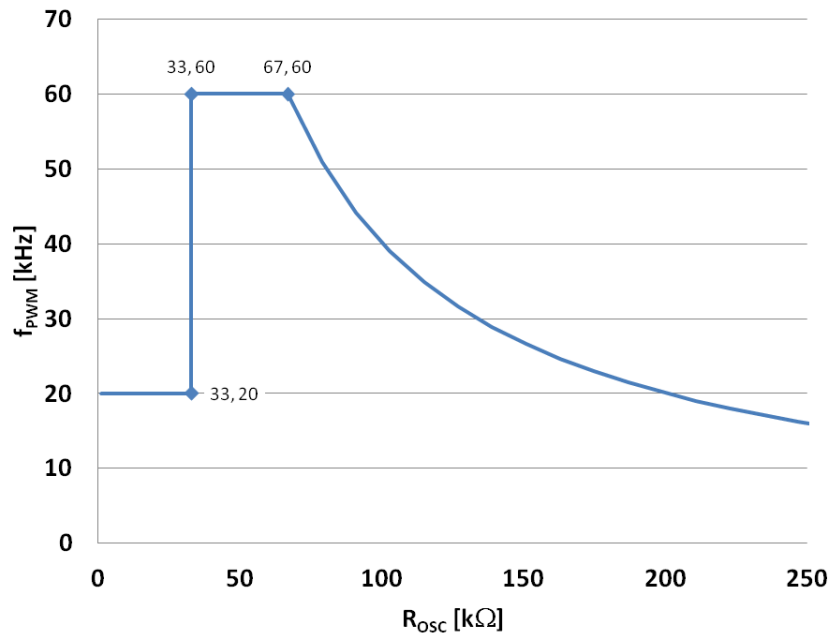


Figure 5. PWM Clock Frequency Setting

Voltage at the OUT pin, that is the gate voltage of an external switching device, is equal to VIN voltage during ON-cycle. It is driven to ground during OFF-cycle. VIN voltages below 15 V can be supplied directly from an external voltage source. Supply voltages of at least 6 V are supported.

DRV110 is able to regulate VIN voltage to 15 V from a higher external supply voltage, V_S , by an internal bypass regulator that replicates the function of an ideal Zener diode. This requires that the supply current is sufficiently limited by an external resistor between V_S and the VIN pin. An external capacitor connected to the VIN pin is used to store enough energy to charge the external switch gate capacitance at the OUT pin. Current limiting resistor size to keep quiescent current less than 1 mA can be calculated by Equation 5.

$$R_S = \frac{V_{S,maxDC} - 15V}{1\text{mA} + I_{Gate,Ave}} \quad (5)$$

Open-drain pull-down path at the STATUS pin is deactivated if either under voltage lockout or thermal shutdown blocks have triggered.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV110APWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to +105	110A	Samples
DRV110PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to +105	110	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV110APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
DRV110PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV110APWR	TSSOP	PW	14	2000	367.0	367.0	35.0
DRV110PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

PW (R-PDSO-G14)

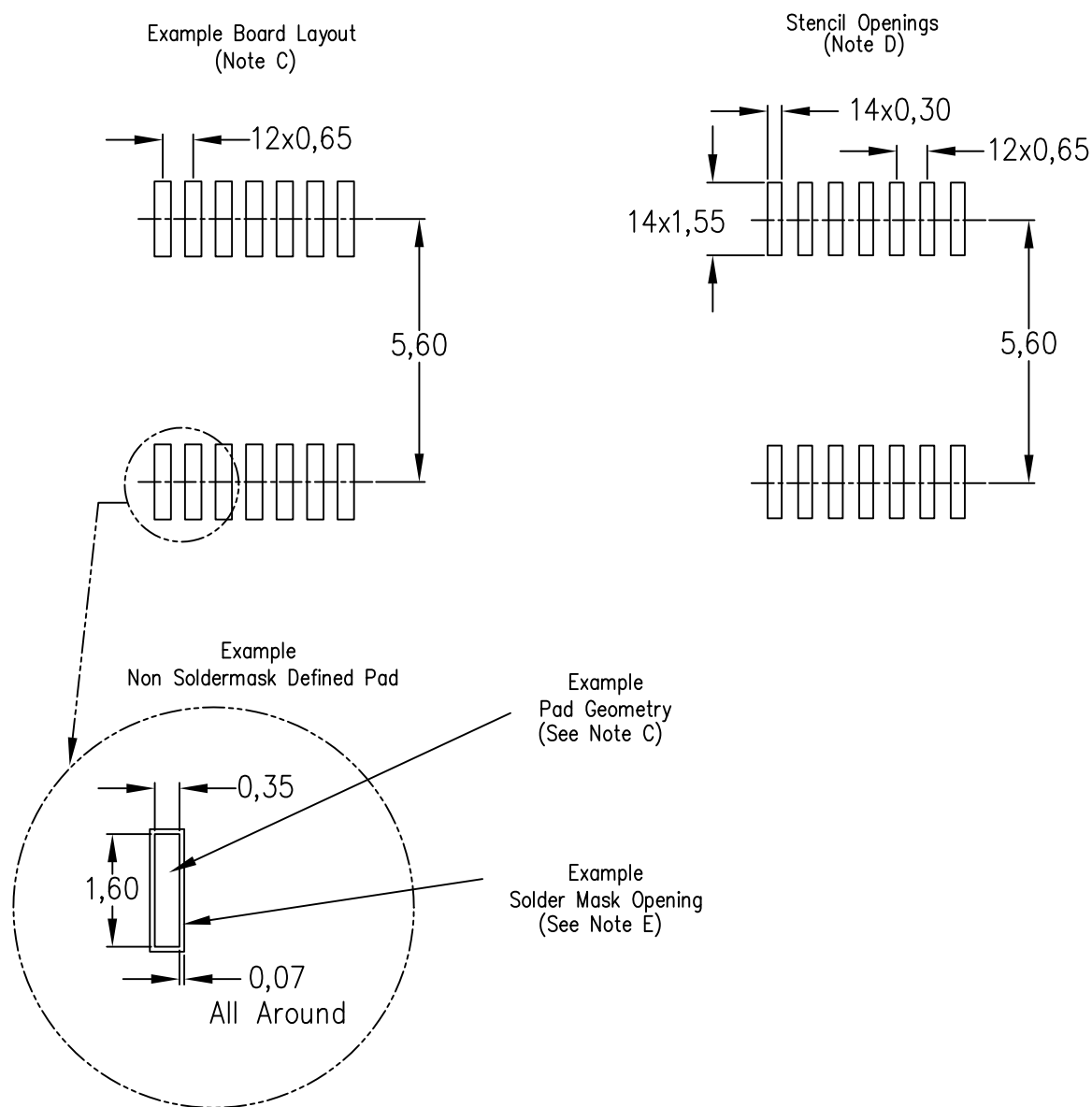
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

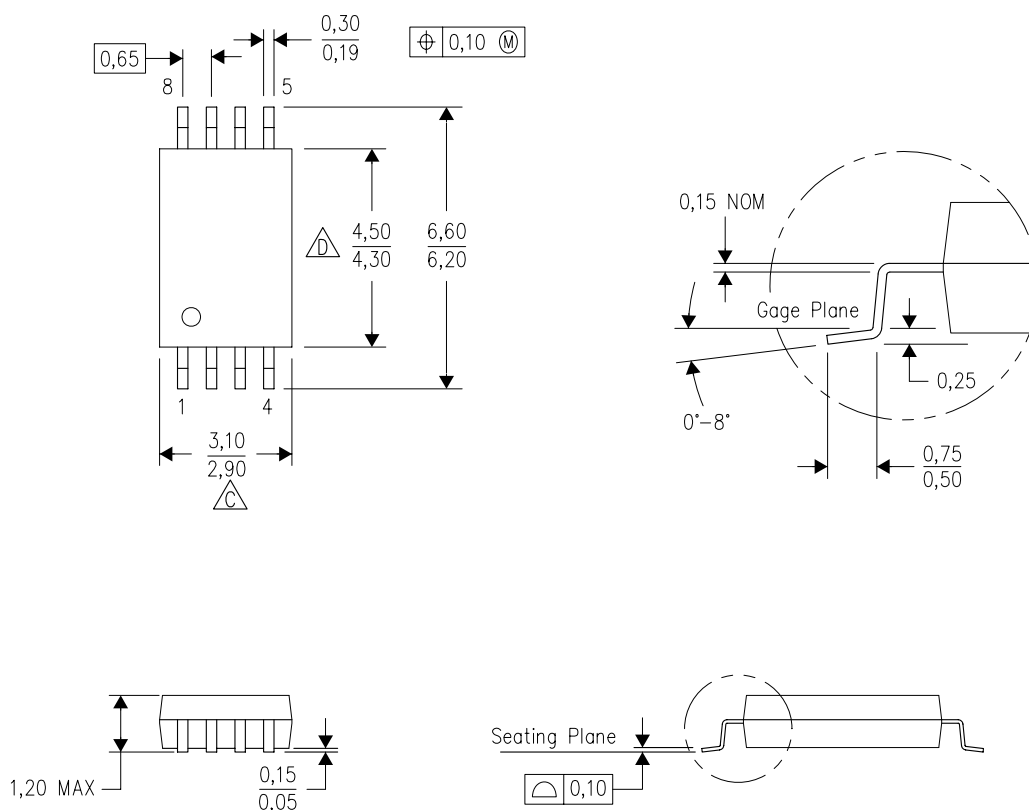


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com