DESCRIPTION

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line to 4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired.

Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3- to 8-line decoder or 1- to 8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

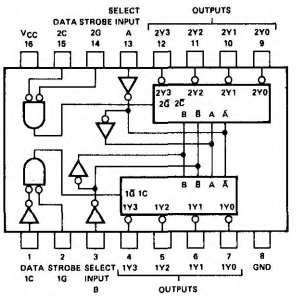
The S54155/N74155 circuits, with totem pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The S54156/N74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the S54155/N74155.

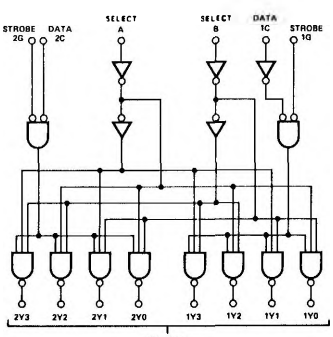
The S54155 and S54156 are characterized for operation over the full military temperature range of -55°C to 125°C the N74155 and N74156 are characterized for operation from 0°C to 70°C.

PIN CONFIGURATION

B,F,W PACKAGE



LOGIC DIAGRAM



TRUTH TABLES

TRUTH TABLES (H = High Level, L = Low Level, X = Irrelevant)

2-LINE TO 4-LINE DECODER OR 1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER TO 1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = Inputs 1G and 2G connected together

RECOMMENDED OPERATING CONDITIONS

	S54155			N74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized Fan-Out from each Output, N: High logic level			20			20	
Low logic level			10			10	
Operating Free-Air Temperature Range, T_A	−55	25	125	0	25	70	°C

	S54156			N74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level Output Current, I_{OL}			16			16	mA
Operating Free-Air Temperature Range, T_A	-55	25	125	0	25	70	°C

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			S54155,N74155 MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = -800μA	V_{IH} = 2V,		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_{IL} = 0.8V,				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V				40	μA
		V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{OS}	Short-circuit output current †	V_{CC} = MAX		S54155	-20		-55	mA
				N74155	-18		-57	
I_{CC}	Supply current	V_{CC} = MAX		S54155		25	35	mA
				N74155		25	40	

ELECTRICAL CHARACTERISTICS (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST CONDITIONS*			S54156,N74156 MIN	TYP**	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 5.5V	V_I = 2V,				250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16mA	V_{IL} = 0.8V,				0.4	V
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4V				40	μA
		V_{CC} = MAX,	V_I = 5.5V				1	mA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4V				-1.6	mA
I_{CC}	Supply current	V_{CC} = MAX		S54156		25	35	mA
				N74156		25	40	

SWITCHING CHARACTERISTICS, V_{CC} = 5V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	S54155 N74155 MIN	S54155 N74155 TYP	S54155 N74155 MAX	S54156 N74156 MIN	S54156 N74156 TYP	S54156 N74156 MAX	UNIT
t_{PLH}	A,B,2C, 1G,or2G	Y	2			13	20		15	23	ns
t_{PHL}	A,B,2C, 1G,or2G	Y	2	C_L = 15pF,		18	27		20	30	ns
t_{PLH}	A or B	Y	3	R_L = 400Ω		21	32		23	34	ns
t_{PHL}	A or B	Y	3			21	32		23	34	ns
t_{PLH}	1C	Y	3			16	24		18	27	ns
t_{PHL}	1C	Y	3			20	30		22	33	ns

* For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

** All typical values are at V_{CC} = 5V, T_A = 25°C.

† Not more than one output should be shorted at a time.

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

TYPICAL APPLICATION DATA

The S54155, N74155, S54156, or N74156 may be used as a dual 2-line to 4-line decoder or a 1-line to 4-line demultiplexer. These applications are identical except as follows:

When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

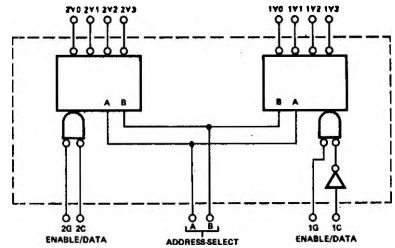
Any of these circuits may also be used as a 3-line to 8-line decoder or a 1-line to 8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

When used as a demultiplexer, the common strobe line serves as the data input.

DUAL 2-LINE TO 4-LINE DECODER/1-TO 4-LINE DEMULTIPLEXER

S54155, N74155, S54156, N74156



3-LINE TO 8-LINE DECODER/1-TO 8-LINE DEMULTIPLEXER

S54155, N74155, S54156, N74156