

Freescale's S32V ADAS Processor Family

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Freescale's Advanced Processor for Next Generation ADAS: S32V234

Freescale introduces a new power and performance optimized heterogeneous processor for Advanced Driver Assistance Systems (ADAS) systems – the S32V family. The processor can process video camera feeds with two image processors from CogniVue and has a high performance GPU with 50GFLOPs of floating point compute power, all while maintaining a ~5W power envelope. The S32V234 is the first member of a family of ADAS processors that bring true automotive quality to ADAS. It is scheduled to sample in 2Q15. Software tools from Green Hill, CogniVue, and Neusoft Automotives will be available at launch.

Introduction

Advanced Driver Assistance Systems (ADAS) is evolving from driver warning systems such as lane departure warning and parking assist, to more important safety tasks that can command control of the car and eventually to fully automated/autonomous vehicles.

The current driver assisted solutions only provide a method of warning the driver of potential threats. Moving to the next level will require the vehicle to take action to control or "co-piloting" the vehicle. Co-piloting will require more computation and more software than the systems today - that is pretty obvious. What may not be obvious is that those systems will have to be *even more reliable* than the automotive chips are today as they will have the lives of the occupants and potentially pedestrians and other drivers at stake – failure is not an option. To reach the level of reliability and safety that will be required of these Advanced Driver Assistance Systems (ADAS) system requires true automotive-grade chips and systems design. Freescale's next generation ADAS system, the S32V family, will meet the computational needs of these next generation safety systems and the reliability requirements as well. In addition, the chip needs a high level of security to protect against intrusions in connected cars.

The S32V family addresses the computational needs of ADAS with a heterogeneous mix of CPUs, GPU, and image cognitive processors. It is only through the mix of heterogeneous processing elements that the chip can meet the compute requirements while maintaining a power envelope of about 5W. Low power is critical because all automotive systems should be passively cooled – it will be difficult for a fancooled system to meet automotive system reliability standards.

Much of the computational performance requirements are driven by the myriad of sensors (image sensors, lidar, radar, etc.) required to actively scan for not only what can be seen, but what cannot. A part of the ADAS sensing will come from optical cameras. Processing the four or more surround cameras will take significant computation capabilities. The S32V234 addresses the optical processing requirements with dual CogniVue APEX2 processors. These processors can handle the four main



automotive cameras (front, back, left side, and right side) and extract features used to classify images. The GPU is used to build a surround view of the environment around the car: building a real-time 3D spatial model of the environment around the car and object and threat calculations. The GPU can also be used as a compute element with around 50GFLOPs of floating point processing.

Automotive ADAS Levels and Reliability

In automotive technology "assisted driving" includes lane departure, blind spot, in-lane vehicle distance warning, automated parking, and emergency braking. For co-piloted, semi-automated driving, these activities extend to active steering control, as well as self parking. Eventually, this progression of automotive safety systems will become capable enough to drive the car without human intervention – the autonomous car. Getting to this final destination requires a few stops along the way an increasing levels of reliability.

Figure 1. ADAS Functionality Timeline



The functional safety standards that automobile manufacturers will need to meet is found in the ISO 26262 standard. Although the standard is limited to automobile only up to a certain weight, this addresses the majority of the potential autonomous market. For this assisted processing ASIL B is the preferred quality level, but for autonomous driving, where failure can be life threatening, the highest level of safety, ASIL D, should be required, see the sidebar for an overview of the standards.

Assisted driving requires optical flow and classification of vision from the stereo or mono front and rear cameras. There is some 2-D/3-D surround imaging required as well, especially for self parking.

Full autonomous driving requires more than just optical sensing – it requires fusion sensing that combines the passive vision processing with active sensing such as radar, lidar, and ultrasonic sensors for full 360° sensing with a 3-D environmental model. Vision is just not sufficient when the control and safety of a car is the requirement. Video camera images can be degraded by low contrast, sun glare, and weather and other environmental conditions. Sensor fusion collects abstract sensor data and confirms objects using the different sensors. It's after the fusion of all the data is made, that the safety system can make a complete decision on the environment around the car and take the appropriate action. This is the most critical part of the safety system and it must be fool proof at the very least. It actually should be "fail operational" where even under a partial failure, the system can perform the minimal capability to keep the occupants safe and not crash the vehicle. It is this control and responsibility that will require



the ultimate in system reliability. In addition, deep learning and advanced machine vision will be required as object classification models will actively evolve over time.

In addition, the sensor fusion processor reliability requirements will likely require some sort of selfchecking architecture where two (or more) processors work in parallel and compare results and actions. If the two processors disagree on actions, then there could be a system failure and this triggers a safe mode of operations. Two S32V234 chips can be placed into a shared memory mode which allows them to see each other's memory and compare results. The goal is to reach a FITS (failure in time) of 10 failures every billion of hours of operation.

Freescale S32V234 Platform

The S32V234, shown in Figure 2, brings a balanced platform approach to ADAS and the next generation of co-piloted systems – the heterogeneous mix of CPU, GPU, and image processors attempts to balance the essential computational requirements without relying on any one element to carry the load. The CPU complex includes a quad-core Cortex-A53 section along with a Cortex-M4 microcontroller. The Cortex-A53 CPU is a 64-bit (ARMv8) core that offers balanced performance supported by ARM's latest instruction set, along with low power and cost-effective die area. To support the reliability requirements of automotive, the processors all have error correcting codes (ECC) protection the data and instructions to the processor caches, the internal 4MB scratchpad memory, and the DRAM memory.

While processors from other vendors screened for automotive safety applications may have higher performance specifications, they often lack the built-in reliability factors, such as ECC, to protect internal circuits from intermittent errors. A voltage spike or even a cosmic ray can alter a DRAM or cache memory location, resulting in temporary erratic operation – this is why critical server processors use ECC memory.



Figure 2. S32V234 ADAS Processor Block Diagram



Freescale S32V ADAS Processor Family

The majority of the heavy lifting on image processing and spatial reconstruction, however, will be performed by the APEX image processors and the GC 3000 GPU. The Cortex-M4 micro is used as an offload processor for low-level tasks and Autosar support.

The APEX2 CL is the 2nd generation image processor comes from leading image IP provider CogniVue. The CogniVue APEX core has two Array Processor Units (APUs) each of which has 32 Computational Units (CUs). Supporting the APEX core is a multi-channel DMA engine and stream DMA engine for external and internal (respectively) data movement, and hardware assist blocks to accelerate some fixed functions. A dedicated sequencer manages processing and data transfer steps. The sequencer also offloads the Coretx-A53 CPUs from having to manage lower level interrupts related to APEX processing. Freescale's chip supports up to 10 video streams, but realistically, will process four 1Mbps (25-30fps) video streams, limited to by memory bandwidth.

The GC3000 GPU comes from graphics IP provider Vivante, and it supports IEEE floating point GPU compute. Vivante has stressed delivering the highest performance per square millimeter of die area. The GPU function will likely be used mostly to its compute functionality, spatial conversion, and 3D space modeling, and less for driving a display. The GC3000 can deliver around 50GFLOPS at 600MHz providing number-crunching capability. One use of the GPU could be to transform radar/lidar polar coordinate descriptions to a Cartesian map of the objects in 3D space around vehicle, as well as calculating motion vectors for each object and the movement of the car itself.

The S32V234 also includes a crypto processor to speed security transaction as security is fast becoming a critical function to protect internal IP as well as protect against external intrusion attacks. The on-chip Image Signal Processor (ISP) is used for camera image preprocessing. The ISP is optimized for functions like dead pixel processing, correction of geometric distortions, High Dynamic Range (HDR) processing, image scaling, color corrections, and others. The ISP has a programmable architecture and can adjust to any kind of image sensor.

There's also an on-chip video codec that supports H.264 video compression and JPEG images, which is fine for the moderate resolution cameras and displays used in automotive. The collection of system I/O includes GigE, PCIe, PD CAN bus, FlexRay automotive bus, etc.

Programming the S32V Family

The primary programming model for the heterogeneous compute functions of the S32V family will be the cross-platform OpenCL API. This API supports multiple architectures and allows the mix of highly parallel compute processors, such as GPUs, along with CPUs. The key advantage of OpenCL is that it is cross-platform and cross architecture API and is not a proprietary interface locked to just one vendor. This advantage allows automotive manufacturer software to be portable across vendors and operating systems.



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Freescale's launch partner for the S32V family include RTOS software provider Green Hills Software and will include Linux and others in the future. Green Hills provides world-class RTOS software to many different industries where dependability, reliability, and predictability are essential.

CogniVue supports its IP with the APEX Core Framework (ACF) development environment for vision application development. The tools afford the developer an abstracted model using a Processing Graph. The ACF tool then interprets and translates the high-level graph into an APU native program. The CogniVue tools are responsible for low-level pipelining of the algorithms on the APEX hardware. Using the abstract graph creation speeds vision development, while the ACF tool turns it into optimized code. The company also provides pre-optimized higher level vision and imaging algorithms and highly optimized low level filter kernels running on the APU.

CogniVue has application libraries for Lane Departure Warning, Forward Collision Warning and Blind-Spot Detection. In addition, CogniVue enables smart backup cameras in automotive with patented software for vision-based object detection and distance estimation.

An additional software partner is Neusoft Automotives, which will deliver image processing algorithms for visual applications; in particular LDW, Pedestrian Detection, and Traffic Sign Recognition.

Security Capabilities

Protecting the intellectual property of vision processor is an important reason to encrypt the instructions and data memories. But even more critical is preventing a hardware attack on the system itself either through physical intrusion or through electronic intrusion. There is no part of a safety critical system that is more important than a component that can control the operating direction of a 2000+ lbs. moving vehicle. The security capability of the S32V family is based on Freescale's experience in network processors and is close to full SHE compliance – lacking only the on-chip storage. The on-chip security features include a crypto security engine to accelerate crypto functions.

Conclusion

When you're in an intelligent car, traveling at sustained speed, you want the most reliable electronics possible controlling the vehicle. That level of trust can only be achieved with parts specifically designed for ultra-reliable system operation. This is the philosophy that Freescale is bringing to future of ADAS – with targeted performance, and unquestioned operational system reliability. The S32V234 is the first in a line of new ADAS processors from Freescale - built for the toughest automotive challenges and an architecture which can scale over time. The S32V family can support the intelligent ADAS requirements for the near future of co-piloted cars and can scale to semi-autonomous control.



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The S32V234 will sample in 2Q15 and Freescale will provide a reference design and SDK. The chip is designed to support ISO 26262 ASIL B standards.