SCLS133E - DECEMBER 1982 - REVISED SEPTEMBER 2003

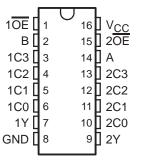
- 3-State Version of 'HC153
- Wide Operating Voltage Range of 2 V to 6 V
- High-Current Inverting Outputs Drive Up To 15 LSTTL Loads
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 9 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max
- Permit Multiplexing From n Lines to One Line
- Perform Parallel-to-Serial Conversion

description/ordering information

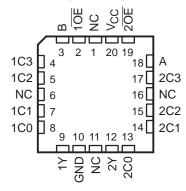
Each of these data selectors/multiplexers contains inverters and drivers to supply full binary decoding data selection to the AND-OR gates. Separate output-control inputs are provided for each of the two 4-line sections.

The 3-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (in the high-impedance state), the low impedance of the single enabled output drives the bus line to a high or low logic level. Each output has its own output-enable (\overline{OE}) input. The outputs are disabled when their respective \overline{OE} is high.

SN54HC253 . . . J OR W PACKAGE SN74HC253 . . . D, DB, N, OR NS PACKAGE (TOP VIEW)



SN54HC253 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

ORDERING INFORMATION

TA	PACKA	GE†	ORDERABLE PART NUMBER	TOP-SIDE MARKING		
	PDIP – N	Tube of 25	SN74HC253N	SN74HC253N		
		Tube of 40	SN74HC253D			
4000 1- 0500	SOIC - D	Reel of 2500	SN74HC253DR	HC253		
-40°C to 85°C		Reel of 250	SN74HC253DT			
	SOP – NS Reel of 2000		SN74HC253NSR	HC253		
	SSOP – DB	Reel of 2000	SN74HC253DBR	HC253		
	CDIP – J	Tube of 25	SNJ54HC253J	SNJ54HC253J		
-55°C to 125°C	CFP – W	Tube of 150	SNJ54HC253W	SNJ54HC253W		
	LCCC - FK	Tube of 55	SNJ54HC253FK	SNJ54HC253FK		

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



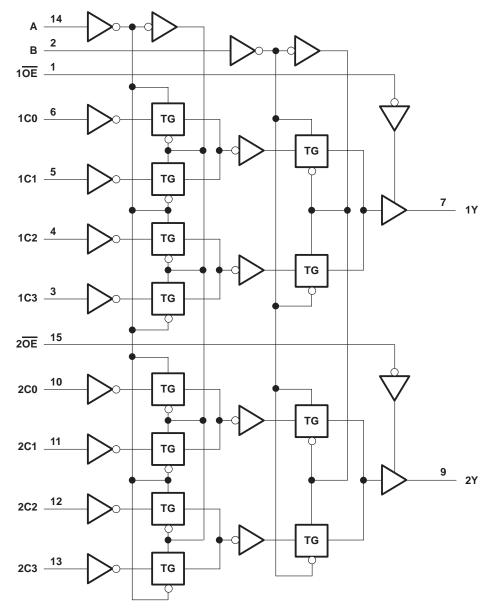
SN54HC253, SN74HC253 DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS SCL\$133E - DECEMBER 1982 - REVISED SEPTEMBER 2003

FUNCTION TABLE

			INPUTS				
SELE	ЕСТ†		DA	ŌĒ	OUTPUT		
В	Α	C0	C1	C2	C3	OE	·
Х	Χ	Х	Χ	Χ	Χ	Н	Z
L	L	L	Χ	Χ	X	L	L
L	L	Н	Χ	Χ	X	L	Н
L	Н	Χ	L	Χ	X	L	L
L	Н	Χ	Н	Χ	X	L	Н
Н	L	Χ	Χ	L	X	L	L
Н	L	Χ	Χ	Н	X	L	Н
Н	Н	Х	Χ	Χ	L	L	L
Н	Н	Χ	Χ	X	Н	L	Н

[†] Select inputs A and B are common to both sections.

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, and W packages.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		0.5	\mbox{V} to 7 \mbox{V}
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see	ee Note 1)		±20 mA
Output clamp current, IOK (VO < 0 or VO > VCO	c) (see Note 1)		±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})			$\pm 25~\text{mA}$
Continuous current through V _{CC} or GND			$\pm 50~\text{mA}$
Package thermal impedance, θ _{JA} (see Note 2):	D package		73°C/W
	DB package		82°C/W
	N package		67°C/W
	NS package		64°C/W
Storage temperature range, T _{stq}		. −65°C 1	to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN	154HC25	53	SI	174HC25	i3	
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		2	5	6	2	5	6	V
		V _{CC} = 2 V	1.5			1.5			
ViH	High-level input voltage	V _{CC} = 4.5 V	3.15			3.15			V
		VCC = 6 V	4.2			4.2			
		V _{CC} = 2 V			0.5			0.5	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35			1.35	V
		V _{CC} = 6 V			1.8			1.8	
VI	Input voltage		0		VCC	0		VCC	V
Vo	Output voltage		0		VCC	0		VCC	V
		V _{CC} = 2 V			1000			1000	
Δt/Δν	Input transition rise/fall time	V _{CC} = 4.5 V			500			500	ns
		V _{CC} = 6 V			400			400	
TA	Operating free-air temperature		-55		125	-40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			.,	Т	A = 25°C	;	SN54H	C253	SN74H	C253	
PARAMETER	TEST CO	ONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
			2 V	1.9	1.998		1.9		1.9		
		$I_{OH} = -20 \mu A$	4.5 V	4.4	4.499		4.4		4.4		
Vон	VI = VIH or VIL		6 V	5.9	5.999		5.9		5.9		V
		$I_{OH} = -6 \text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -7.8 \text{ mA}$	6 V	5.48	5.8		5.2		5.34		
			2 V		0.002	0.1		0.1		0.1	
		$I_{OL} = 20 \mu A$	4.5 V		0.001	0.1		0.1		0.1	
VoL	$V_I = V_{IH} \text{ or } V_{IL}$		6 V		0.001	0.1		0.1		0.1	V
		I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 7.8 \text{ mA}$	6 V		0.15	0.26		0.4		0.33	
lį	$V_I = V_{CC}$ or 0		6 V		±0.1	±100		±1000		±1000	nA
loz	VO = VCC or 0		6 V		±0.01	±0.5		±10		±5	μΑ
Icc	$V_I = V_{CC}$ or 0,	IO = 0	6 V			8		160		80	μΑ
Ci			2 V to 6 V		3	10		10		10	pF

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	_V	T,	4 = 25°C	;	SN54H	C253	SN74H	IC253																
PARAMETER	(INPUT)	(OUTPUT)	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT															
			2 V		62	150		225		190																
	A or B	Any Y	4.5 V		19	30		45		38																
			6 V		16	26		38		32																
t _{pd}			2 V		54	126		210		175	ns															
	Data (Any C)	Y	Υ	4.5 V		16	28		42		35															
	(Ally O)		6 V		13	23		36		30																
			2 V		28	100		150		125																
t _{en}	ŌĒ	Y	4.5 V		11	20		30		25	ns															
			6 V		9	17		26		21																
		Y	Y	Y	Y	Y	2 V		21	135		203		170												
^t dis	ŌĒ						Υ	Υ	Y	Y	Υ	4.5 V		14	30		45		38	ns						
			6 V		12	35		38		31																
			2 V		28	60		90		75																
t _t		Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Υ	Y	Y	Y	4.5 V		8	12		18		15	ns
			6 V		6	10		15		13																

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switching characteristics over recommended operating free-air temperature range, C_L = 150 pF (unless otherwise noted) (see Figure 1)

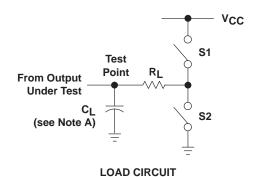
545445755	FROM	то	.,	T	λ = 25°C	;	SN54H	C253	SN74H	C253															
PARAMETER	(INPUT)	(OUTPUT)	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT														
			2 V		76	235		355		295															
	A or B	Any Y	4.5 V		23	47		71		59															
			6 V		20	41		60		51															
^t pd		Y	Υ	2 V		68	220		335		275	ns													
	Data (Any C)			4.5 V		20	44		67		55														
	(Ally O)		6 V		17	38		57		51															
		Y	2 V		44	185		280		230															
^t en	ŌĒ		Υ	Y	Υ	Y	Y	Y	Y	Υ	Y	Y	Υ	Υ	Y	4.5 V		16	37		56		46	ns	
		Y	6 V		14	32		48		40															
			Y	Υ .	Y	Y	Y	Y	Y	2 V		45	210		315		265								
t _t										Y	Y	Y	Y	Y	Y	Y	Υ	Υ	Y	Y	Y	Υ	Υ	Υ	4.5 V
			6 V		13	36		53		45															

operating characteristics, $T_A = 25^{\circ}C$

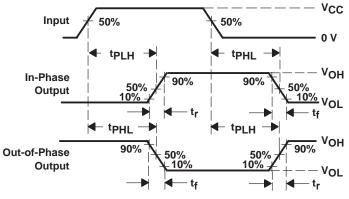
	PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance per multiplexer	No load	45	pF

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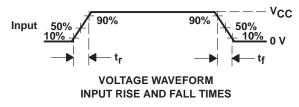
PARAMETER MEASUREMENT INFORMATION

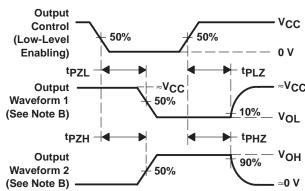


PARAI	METER	RL	CL	S1	S2
	tPZH	1 k Ω	50 pF	Open	Closed
^t en	t _{en} t _{PZL}		or 150 pF	Closed	Open
4	tPHZ		50 pF	Open	Closed
^t dis	tPLZ	1 k Ω	50 pr	Closed	Open
t _{pd} or	t _{pd} or t _t		50 pF or 150 pF	Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES





VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_O = 50 Ω , t_f = 6 ns.
 - D. The outputs are measured one at a time with one input transition per measurement.
 - E. tpLZ and tpHZ are the same as tdis.
 - F. tpzL and tpzH are the same as ten.
 - G. tpLH and tpHL are the same as tpd.

Figure 1. Load Circuit and Voltage Waveforms







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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Sample
5962-88682012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	-55 to 125	5962- 88682012A SNJ54HC 253FK	Sample
5962-8868201EA	ACTIVE	CDIP	J	16	1	TBD	Call TI	Call TI	-55 to 125	5962-8868201EA SNJ54HC253J	Sample
SN54HC253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN54HC253J	Sample
SN74HC253D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sample
SN74HC253DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Sampl
SN74HC253N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC253N	Sampl





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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Top-Side Markings	Samples
SN74HC253NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC253N	Samples
SN74HC253NSR	ACTIVE	so	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Samples
SN74HC253NSRE4	ACTIVE	so	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Samples
SN74HC253NSRG4	ACTIVE	so	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC253	Samples
SNJ54HC253FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 88682012A SNJ54HC 253FK	Samples
SNJ54HC253J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-8868201EA SNJ54HC253J	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): Tl's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, Tl Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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⁽⁴⁾ Only one of markings shown within the brackets will appear on the physical device.



PACKAGE OPTION ADDENDUM

24-Jan-2013

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54HC253, SN74HC253:

Catalog: SN74HC253

Automotive: SN74HC253-Q1, SN74HC253-Q1

● Enhanced Product: SN74HC253-EP, SN74HC253-EP

Military: SN54HC253

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





Α0	Dimension designed to accommodate the component width
	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

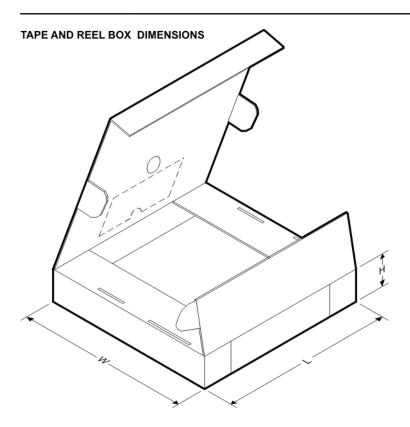
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC253DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74HC253DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HC253NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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*All dimensions are nominal

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Device	Package Type	Package Drawing	Pins SPQ		Length (mm)	Width (mm)	Height (mm)	
SN74HC253DBR	SSOP	DB	16	2000	367.0	367.0	38.0	
SN74HC253DR	SOIC	D	16	2500	333.2	345.9	28.6	
SN74HC253NSR	SO	NS	16	2000	367.0	367.0	38.0	

14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDS0-G16)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.

D. Falls within JEDEC MO-150

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