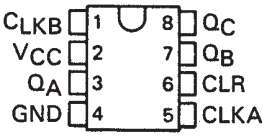
SDLS182 – DECEMBER 1983 – REVISED MARCH 1988

- **'LS56 Performs 50 to 1 Frequency Division (5 to 1, 5 to 1, and 10 to 1)**
- **'LS57 Performs 60 to 1 Frequency Division (6 to 1, 5 to 1, and 10 to 1)**
- **Available in P or JG package (two P or JG Packages Fit in a Single 16-pin Socket)**
- **Maximum Clock Frequency 25 MHz Typical**

SN54LS56, SN54LS57 . . . JG PACKAGE
SN74LS56, SN74LS57 . . . JG OR P PACKAGE

(TOP VIEW)



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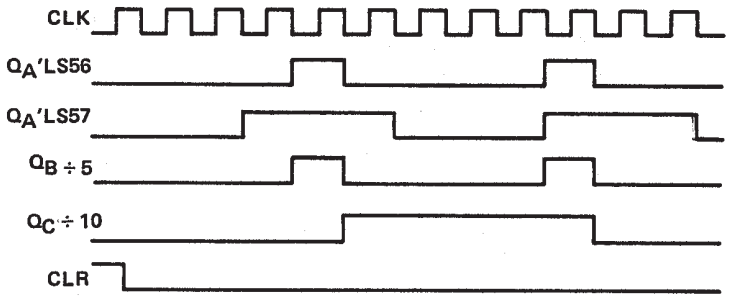
description

These frequency dividers are particularly useful in generating one second or one hour timing pulses from 50 Hz (European standard frequency) or 60 Hz (United States standard frequency). 50 to 1 frequency division is accomplished in the 'LS56 by connecting output Q_A to input CLKB. 60 to 1 frequency division in the 'LS57 is accomplished in the same way. More universal capabilities are evidenced by the 25 MHz typical f_{max} and the almost limitless frequency division possibilities when used in cascade. Two 'LS56 packages may be interconnected to give frequency division of 2500 to 1, 625 to 1, 100 to 1, etc. Two 'LS57 packages can be connected to generate frequency divisions of 3600 to 1, 1800 to 1, 900 to 1 etc.

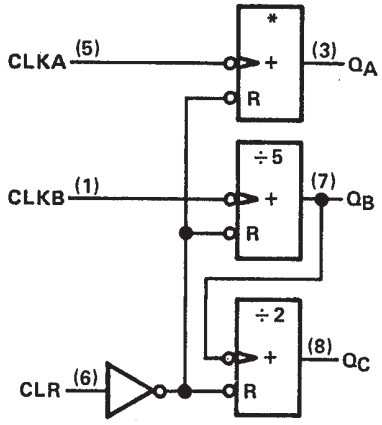
The 'LS56 and 'LS57 frequency dividers consist of three separate counters, A, B, and C on a single monolithic substrate. The A counter divides by 5 to 1 in the 'LS56 and by 6 to 1 in the 'LS57. The B counter divides by 5 to 1 in both devices and is internally tied to the C counter which divides by 2 to 1. The resulting C counter output is 10 to 1. Both the 'LS56 and 'LS57 feature a clear pin which is common to all three counters, A, B, and C. When the clear pin is low, the counters are enabled. When the clear is high, the counters are disabled and their outputs are set to a low-level.

All three counters, A, B, and C trigger on the high-to-low transition of the clock input. All output waveforms are symmetrical except for the 5 to 1 outputs (A and B of the 'LS56 and B of the 'LS57). See the output waveform drawings below.

input and output waveforms



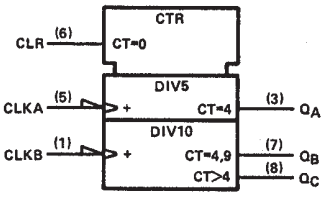
logic diagram (positive logic)



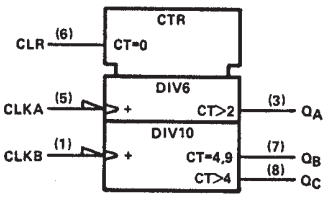
* 'LS56 ÷5
'LS57 ÷6

logic symbols†

'LS56

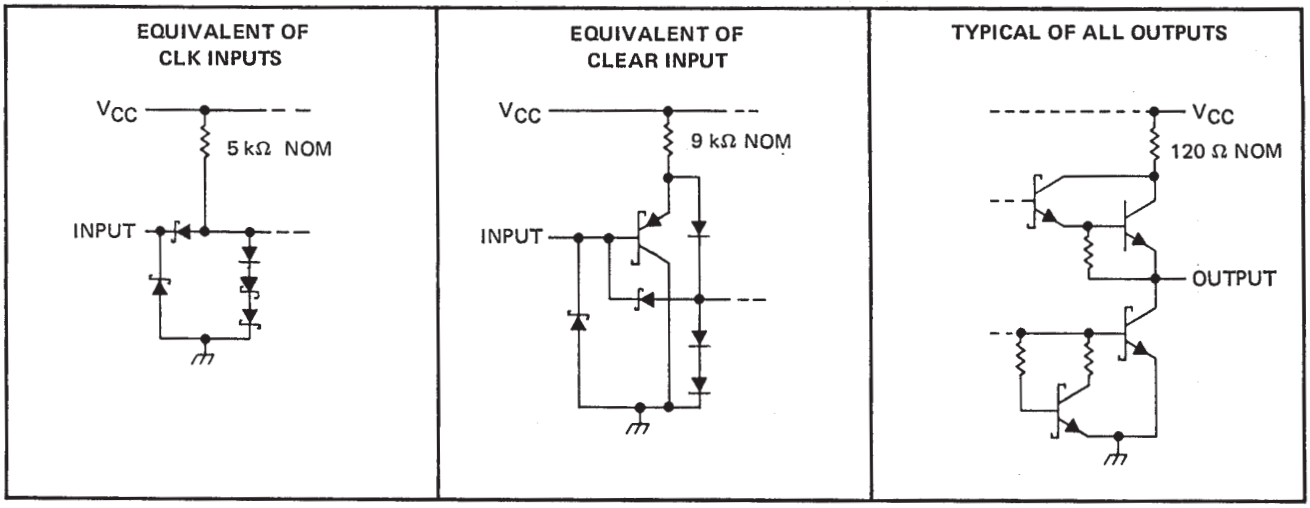


'LS57



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: CLR . . . . . 7 V
CLKA, CLKB . . . . . 5.5 V
Operating free-air temperature range: SN54LS' . . . . . −55°C to 125°C
SN74LS' . . . . . −0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			−1			−1	mA
I_{OL}	Low-level output current			8			16	mA
f_{clock}	Clock frequency	0		15	0		15	MHz
t_r, t_f	Rise and fall time of clock			50			50	ns
t_w	Pulse width of clock or clear	30			30			ns
t_{su}	Clear inactive state set-up time	25			25			ns
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS' MIN	SN54LS' TYP‡	SN54LS' MAX	SN74LS' MIN	SN74LS' TYP‡	SN74LS' MAX	UNIT
V_{IK}		V_{CC} = MIN, I_I = – 18 mA				– 1.5			– 1.5	V
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OH} = – 1 mA	2.5	3.4		2.7	3.4		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	
I_I	CLKA, CLKB	V_{CC} = MAX	V_I = 5.5 V			0.2			0.2	mA
	CLR		V_I = 7 V			0.1			0.1	
I_{IH}	CLKA, CLKB	V_{CC} = MAX, V_I = 2.7 V				80			80	μA
	CLR					20			20	
I_{IL}	CLKA, CLKB	V_{CC} = MAX, CLR = 0 V, V_I = 0.4 V				– 3.2			– 3.2	mA
	CLR					– 0.2			– 0.2	
I_{OS}§		V_{CC} = MAX, CLR = 0 V, V_O = 0 V		– 20		– 100	– 20		– 100	mA
I_{CC}		V_{CC} = MAX, See Note 2			17	30		17	30	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured by applying 4.5 V to the CLR pin with all other inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS56 MIN	'LS56 TYP	'LS56 MAX	'LS57 MIN	'LS57 TYP	'LS57 MAX	UNIT
f_{max}	CLKA	Q_A	R_L = 1 kΩ, C_L = 30 pF	15	25		15	25		MHz
f_{max}	CLKB	Q_B, Q_C		15	25		15	25		MHz
t_{PLH}	CLKB	Q_B			8	15		8	15	ns
t_{PHL}					14	25		14	25	ns
t_{PLH}¶	CLKB	Q_C			18	30		18	30	ns
t_{PHL}¶					24	35		24	35	ns
t_{PLH}	CLKA	Q_A			12	20		14	25	ns
t_{PHL}					14	25		18	30	ns
t_{PHL}	CLR	Q_A			17	30		17	30	ns
t_{PHL}	CLR	Q_B			17	30		17	30	ns
t_{PHL}	CLR	Q_C			17	30		17	30	ns

¶Times measured from CLKB to output Q_C are taken with output Q_B unloaded.
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LS56P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
SN74LS57P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
SN74LS57P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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