PLESSEY
SEMICONDUCTORS

SP1600 SERIES
ECL III

SP1670B (HIGH Z)
SP1671B (LOW Z)
MASTER/SLAVE TYPE D FLIP-FLOP

The SP1670B is a Type D Master-Slave Flip-Flop designed for use in high speed digital applications. Master-slave construction renders the SP1670B relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the Master portion of the flip-flop. The data present in the Master is transferred to the Slave when clock inputs (C1 OR C2) are taken from a low to a high level. In other words, the output state of the flip-flop changes on the positive transition of the clock pulse.

While either C1 OR C2 is in the high state, the Master (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

Input pulldown resistors eliminate the need to tie unused inputs to V_{EE}.

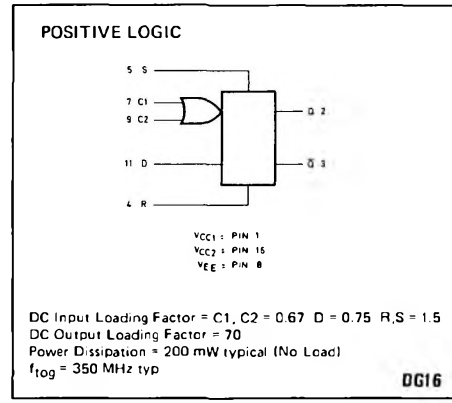


Fig. 1 Logic diagram

FEATURES

- Toggle Frequency > 300 MHz
- MECL/PECL II and MECL 10000-Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation

APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems

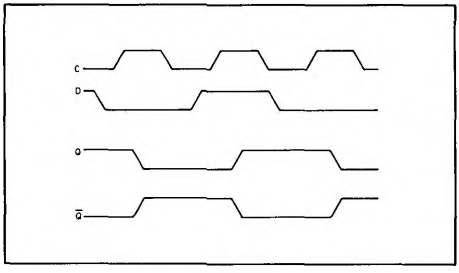


Fig. 2 Timing diagram

TRUTH TABLE				
R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↗	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↗	H
L	L	H	H	Q_n

ϕ = Don't Care
ND = Not Defined
C = C1 + C2

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $\lvert V_{CC} - V_{EE} \rvert$	8V
Base input voltage	0V to V_{EE}
O/P source current	< 40mA
Storage temperature	−55°C to +150°C
Junction operating temp.	< +125°C

ELECTRICAL CHARACTERISTICS

This PECL III circuit has been designed to meet the d.c. specifications shown in the characteristics table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear ft/min is maintained. Outputs are terminated through a 50Ω resistor to −2.0 volts.

@ Test Temperature	TEST VOLTAGE VALUES (V)				
	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	−0.840	−1.870	−1.135	−1.500	−5.2
+25°C	−0.810	−1.850	−1.095	−1.485	−5.2
+75°C	−0.720	−1.830	−1.035	−1.460	−5.2

Characteristic	Symbol	Pin Under Test	SP1670B Test Limits							TEST VOLTAGE APPLIED TO PINS LISTED BELOW:							
			0°C		+25°C		+75°C										
			Min	Max	Min	Max	Min	Max	Unit	$V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	P_1	P_2	P_3	OV
Power Supply Drain Current	I_E	–	–	–	–	48	–	–	mA	9,7	–	–	–	8	–	–	–	1,16
Input Current	$I_{in\ H}$	4	–	–	–	550	–	–	µA	4	–	–	–	8	–	–	–	1,16
		5	–	–	–	550	–	–		5	–	–	–		–	–	–	
		9	–	–	–	250	–	–		9	–	–	–		–	–	–	
		7	–	–	–	250	–	–		7	–	–	–		–	–	–	
		11	–	–	–	270	–	–		11	–	–	–		–	–	–	
	$I_{in\ L}$	4	–	–	0.5	–	–	–	µA	9	4	–	–	8	–	–	–	1,16
		5	–	–	–	–	–	–		9	5	–	–		–	–	–	
		9	–	–	–	–	–	–		7	9	–	–		–	–	–	
		7	–	–	–	–	–	–		9	7	–	–		–	–	–	
		11	–	–	–	–	–	–		9	11	–	–		–	–	–	
Logic "1" Output Voltage	V_{OH}	2	−1.000	−0.840	−0.960	−0.810	−0.900	−0.720	V	–	4,7,11	–	–	8	9	5	–	1,16
		3								11	5,9	–	–		7	4	–	
		2								11	5,7	–	–		4	9	–	
		3								–	4,9,11	–	–		5	7	–	
Logic "0" Output Voltage	V_{OL}	2	−1.870	−1.635	−1.850	−1.620	−1.830	−1.595	V	11	5,7	–	–	8	9	4	–	1,16
		3								–	4,9,11	–	–		7	5	–	
		2								–	4,7,11	–	–		5	9	–	
		3								11	5,9	–	–		4	7	–	
Logic "1" Threshold Voltage	V_{OHA}	2	−1.020	–	−0.980	–	−0.920	–	V	–	4,7,11	–	–	8	9	–	5	1,16
		3		–		–		–		11	5,9	–	–		7	–	4	
		2		–		–		–		11	5,7	–	–		4	–	9	
		3		–		–		–		–	4,9,11	–	–		5	–	7	
		2		–		–		–		–	5,7	11	–		4	9	–	
		3		–		–		–		–	4,9	–	11		5	7	–	
Logic "0" Threshold Voltage	V_{OLA}	2	–	−1.615	–	−1.600	–	−1.575	V	11	5,7	–	–	8	9	–	4	1,16
		3	–		–		–			–	4,9,11	–	–		7	–	5	
		2	–		–		–			–	4,7,11	–	–		5	–	9	
		3	–		–		–			11	5,9	–	–		4	–	7	
		2	–		–		–			–	4,7	–	11		5	9	–	
		3	–		–		–			–	5,9	11	–		4	7	–	
Switching Parameters			Min	Max	Min	Max	Min	Max						−3.2 V				+2.0 V
Clock to Output Delay	t_{0+2+}	9,2	1.0	2.5	1.1	2.5	1.1	2.7	ns	–	–	–	–	8	–	–	–	1,16
(See Figure 5)	t_{0-2-}	9,2								–	–	–	–		–	–	–	
	t_{0+3-}	9,3								–	–	–	–		–	–	–	
	t_{0-3+}	9,3								–	–	–	–		–	–	–	
Set to Output Delay	t_{5+2+}	5,2								–	–	–	–		–	–	–	
(See Figure 6)	t_{5+3-}	5,3								–	–	–	–		–	–	–	
Reset to Output Delay	t_{4+2-}	4,2								–	–	–	–		–	–	–	
(See Figure 6)	t_{4+3-}	4,3								–	–	–	–		–	–	–	
Output Rise Time	$t_{2+,3+}$	2,3	0.9	2.5	1.0	2.5	1.0*	2.7		–	–	–	–		–	–	–	
Fall Time	$t_{2-,3-}$	2,3	0.5	1.9	0.6	1.9	0.6	2.1		–	–	–	–		–	–	–	
(See Figure 6)																		
Set Up Time	$t_{s\ 1^{+}}$	2	–	–	–	0.4	–	–		–	2	–	–		–	–	–	
(See Figure 7)	$t_{s\ 0^{+}}$	2	–	–	–	0.5	–	–		–	2	–	–		–	–	–	
Hold Time	$t_{h\ 1^{+}}$	2	–	–	–	0.3	–	–		–	2	–	–		–	–	–	
(See Figure 7)	$t_{h\ 0^{+}}$	2	–	–	–	0.5	–	–		–	2	–	–		–	–	–	
Toggle Frequency (See Figure 8)	f_{Tog}	2	270	–	300	–	270	–	MHz	–	–	–	–		–	–	–	–

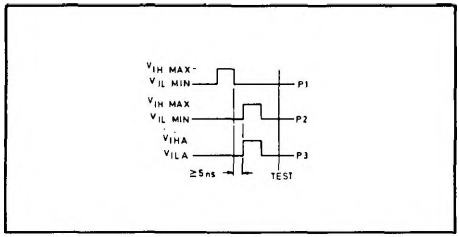


Fig. 3 Static test pulses

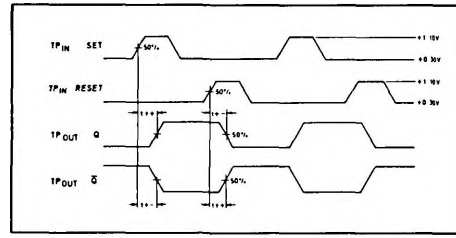


Fig. 6 Set/reset delay waveform at +25°C

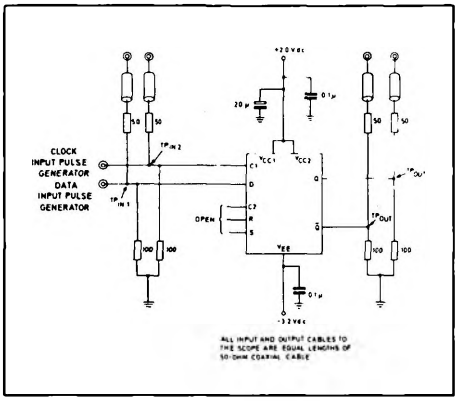
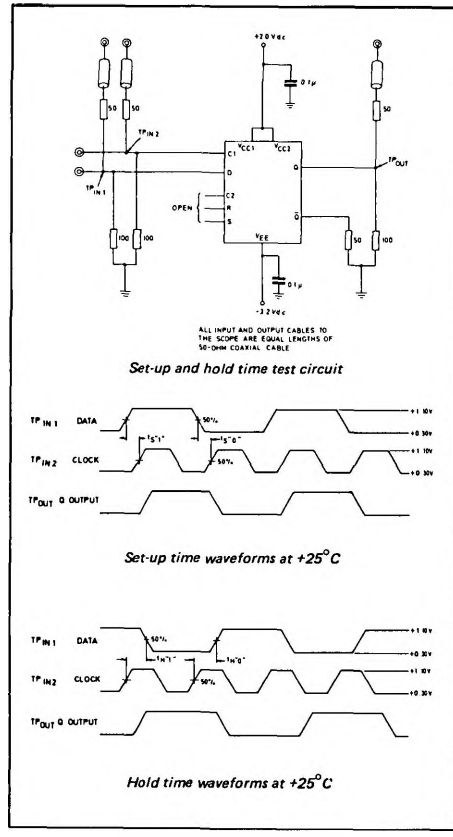


Fig. 4 Propagation delay test circuit



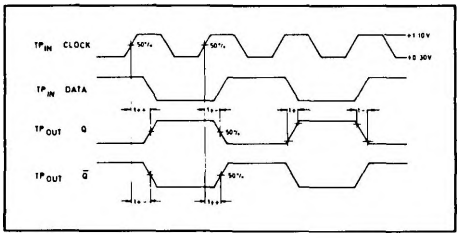


Fig. 5 Clock delay waveforms at +25°C

Fig. 7 Set-up and hold time test circuit

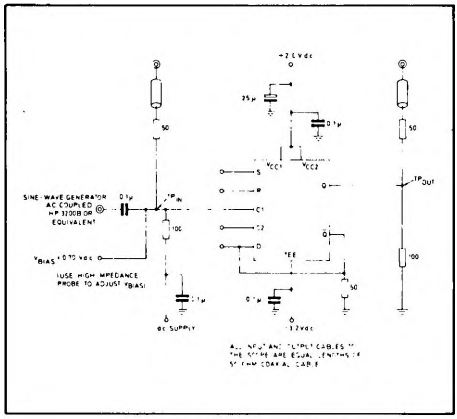


Fig. 8 Toggle frequency test circuit

OPERATING NOTES

Set up time is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data (D) input.

Hold time is the minimum time after the positive transition of the clock (C) that information must remain unchanged at the data (D) input.

V_{Bias} is defined by the test circuit Fig.8 and by the waveform in Fig.9.

Figures 10 and 11 illustrate minimum clock pulse width recommended for reliable operation of the SP1670B.

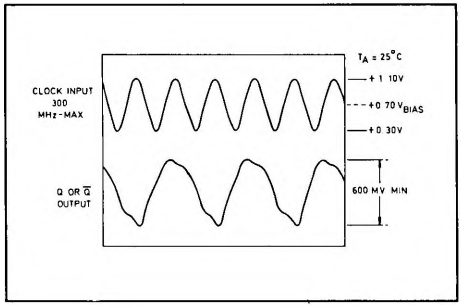


Fig. 9 Toggle frequency waveforms

The maximum toggle frequency of the SP1670B has been exceeded when either:

1. The output peak-to-peak voltage swing falls below 600 millivolts.
   OR
2. The device ceases to toggle (divide by two).

Temperature	0°C	+25°C	+75°C
V_{Bias}	+0.675V	+0.700V	+0.750V

Table 1 Variation of V_{Bias} with temperature

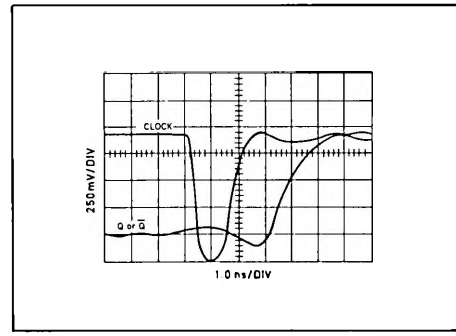


Fig. 10 Minimum 'downtime' to clock output load = 50Ω

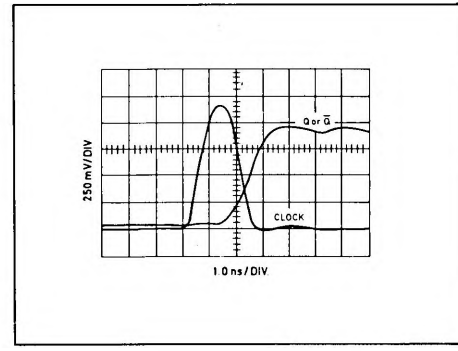


Fig. 11 Minimum 'up time' to clock output load = 50Ω

Operation of the Master-Slave Type D Flip-Flop

In the circuit of Figure 14 assume that initially Q, C, R, S and D are at 0 levels and that $\overline{Q}$ is at the 1 level. Since the clock is low, transistors TR3 and TR22 are conducting. In the slave section only transistors TR25 and TR26 are in series with TR22. The output of the slave section is fed back to these two transistors in order to form a latch. Thus, when the clock is low, the output state of the slave is maintained. In the master section, the current path is through TR3 and TR9.

Now assume that the data input goes high. The high-input signal on the base of TR4 causes it to conduct, and TR9 to turn off. The voltage drop across resistor RC1 causes a low-state voltage on the base and therefore on the emitter of TR11. Since there is essentially no current flow through RC2, the base of transistor TR10 is in a high state. This is reflected in the emitter, and in turn is transferred to the base of TR6. TR6 is biased for conduction but, since there is no current path, does not conduct.

Now allow the clock to go high. As the clock signal rises, transistor TR2 turns on and transistor TR3 turns off. This provides a current path for the common-emitter transistors TR5, TR6, TR7, and TR8. Since the bases of all these devices except TR6 are in the low state, current flow is through TR6. This maintains the base and emitter of TR11 low, and the base and emitter of TR10 high. The high state on TR10 is transferred to TR23 of the slave section. As the clock continues to rise TR21 begins to turn on and TR22 to turn off. (Reference voltages in the master and slave units are slightly offset to ensure prior clocking of the master section.) With transistor TR21 conducting and the base of TR23 in a high state, the current path now includes TR21, TR23, and resistor RC3. The voltage drop across the resistor places a low state voltage on the base, and therefore the emitter, of TR30. The lack of current flow through RC4 causes a high state input to the base of TR29. These states are fed back to the latch transistors, TR25 and TR26.

As the clock voltage falls, transistor TR21 turns off and TR22 turns on. This provides a current path through the latch transistors, locking-in the slave output.

In the master section the falling clock voltage turns on transistor TR3 and turns off TR2. This enables the input transistor TR4 so that the master section will again track the D input.

The separation of thresholds between the master and slave flip-flops is caused by R8. The current through this resistor produces an offset between the thresholds of the transistor pairs TR2:TR3 and TR21:TR22. This offset disables the D input of the master flip-flop prior to the enabling of the information transfer from master to slave via transistors TR23 and TR28. This disabling operation prevents false information from being transferred directly from master to slave during the clock transition, particularly if the D input changes at this time (such as in a counting operation where the $\overline{Q}$ output is tied back to D). The offsetting resistor also allows a relatively slow-rising clock waveform to be used without the danger of losing information during the transition of the clock.

The set and reset inputs are symmetrically connected. Therefore, their action is similar although results are opposite. As a logic 1 level is applied to the S input transistor, TR2 begins to conduct because its base is now being driven through TR19 which is in turn connected to S. Transistor TR5 is now on and the feedback devices TR6 and TR7 latch this information into the master flip-flop. A similar action takes place in the slave with transistors TR21, TR24, TR25, and TR26.

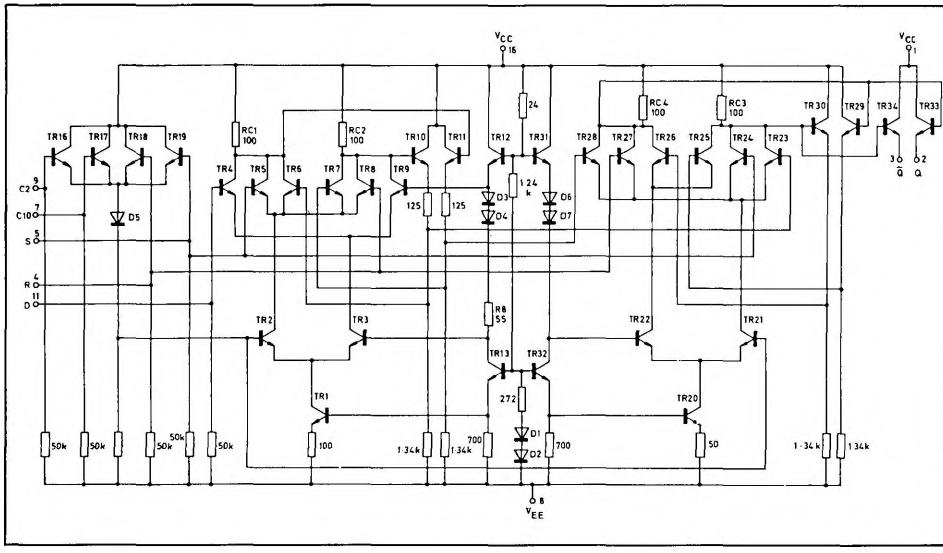


Fig. 12 SP1670 circuit diagram