

VPS13

CRT Display Video Output Amplifier, High-Voltage/Wideband Amplifier

Features

• High output voltage and wide bandwidth; optimal for use in f_H (horizontal deflection frequency) = 100 kHz class monitors.

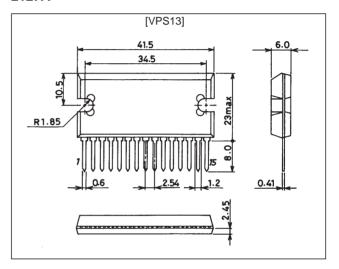
 $(f = 130 \text{ MHz} - 3 \text{ dB at V}_{OUT} = 40 \text{ Vp-p})$

• SIP molded 15-pin package houses three amplifier channels.

Package Dimensions

unit: mm

2127A



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
	V _{CC} max		90	V
Maximum supply voltage	V _{BB} max		15	V
Allowable power dissipation	Pd max	With an ideal heat sink at Tc = 25°C	30	W
Maximum junction temperature	Tj max		150	°C
Maximum case temperature	Tc max		100	°C
Storage temperature	Tstg		-20 to +110	°C

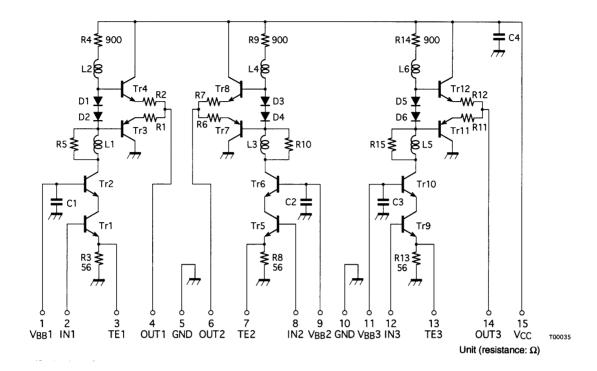
Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
December of the second	V _{CC}		80	V
Recommended supply voltage	V _{BB}		10	٧

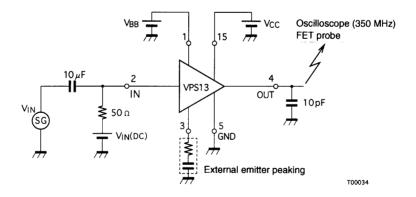
Electrical Characteristics at $Ta = 25^{\circ}C$ (for a single channel)

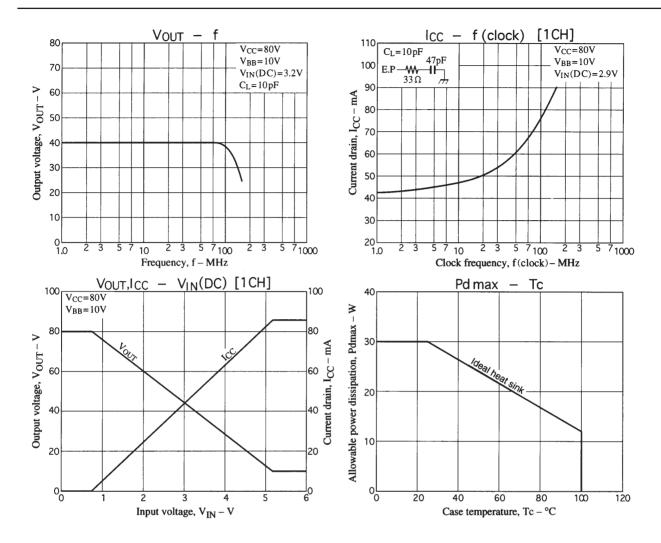
Parameter	Cumphal	Conditions	Ratings			Unit
Falametei	Symbol Conditions		min	typ	max	
Frequency band (-3 dB)	f _C	$V_{CC} = 80 \text{ V}, V_{BB} = 10 \text{ V}, C_L = 10 \text{ pF}$ $V_{IN} (DC) = 3.2 \text{ V}, V_{OUT} (p-p) = 40 \text{ V}$		130		MHz
Impulse response	t _r	V _{CC} = 80 V, V _{BB} = 10 V, C _L = 10 pF		3.5		ns
	t _f	V_{IN} (DC) = 3.2 V, V_{OUT} (p-p) = 40 V		2.9		ns
Voltage gain	VG (DC)		13	15	17	double
Current drain	I _{CC} (1)	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 2.9 V, f = 10 MHz clock, C_L = 10 pF, V_{OUT} (p-p) = 40 V		47		mA
	I _{CC} (2)	$V_{CC} = 80 \text{ V}, V_{BB} = 10 \text{ V}, V_{IN} \text{ (DC)} = 2.9 \text{ V}, \\ f = 130 \text{ MHz clock, } C_L = 10 \text{ pF}, V_{OUT} \text{ (p-p)} = 40 \text{ V}$		85		mA

Internal Equivalent Circuit



Test Circuit (for a single channel)





Thermal Design

Since the VPS13 includes three channels as shown in the circuit diagram on page 2, we first consider a single channel. The chip temperature of each transistor under actual operating conditions is determined using the following formula.

$$Tj = (Tri) = \theta j-c (Tri) \times Pc (Tri) + \Delta Tc + Ta (^{\circ}C) \dots (1)$$

 θ j-c (Tri): Thermal resistance of an individual transistor Pc(Tri): Collector loss for an individual transistor

 ΔTc : Case temperature rise Ta : Ambient temperature

The θ j-c (Tri) for each chip is: θ j-c (Tr1) = 35°C/W

$$\theta$$
j-c (Tr2) to (Tr4) = 30°C/W....(2)

Although the loss for each transistor in a video pack varies with frequency and is not uniform, if we assume the maximum operating frequency, f = 130 MHz (clock), then the chip with the largest loss will be transistor 3 (Tr3) of the emitter-follower stage. From the Pd-f (clock) figure we see that loss will be 22% of the total loss for a single channel:

Pc (emitter-follower stage)_(f = 130 MHz) = Pd (1ch)
$$_{(f = 130 \text{ MHz})} \times 0.22 \text{ [W]}$$
 (3)

Here, we must select a heat sink with a capacity θ h such that the Tj of these transistors does not exceed 150°C. Equation (4) below gives the relationship between θ h and Δ Tc.

$$\Delta Tc = Pd (Total) \times \theta h$$
(4)

The required θ h is calculated using this equation and equation (1).

VPS13 Thermal Design Example

Conditions: Using an $f_H = 100 \text{ kHz}$ class monitor, $f_V = 130 \text{ MHz}$ (clock)

$$V_{CC} = 80 \text{ V}, V_{BB} = 10 \text{ V}, V_{OUT} = 40 \text{ Vp-p } (C_L = 10 \text{ pF})$$

Here we consider the case where this class of monitor is operated up to $Ta = 60^{\circ}C$ at a maximum clock frequency of f = 130 MHz.

As mentioned previously, the chip with the largest loss is transistor 3 (Tr3) of the emitter-follower stage. Determining that value gives:

Pc (emitter-follower stage) =
$$6.8 \times 0.22 \approx 1.5$$
 [W](5)

Now, determine ΔT_i by substituting the value for θ_i -c in equation (5).

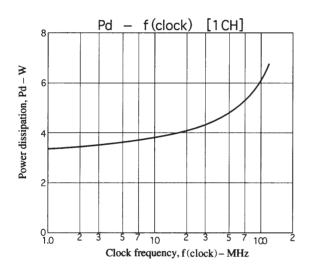
$$\Delta T_i = 1.5 \times 30 = 45 \, [^{\circ}C]$$

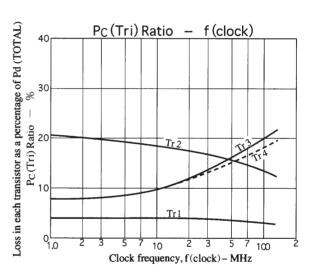
Here, $\Delta Tj < 50^{\circ}C$, and we need only consider cases where $Tc < 100^{\circ}C$. Therefore, we must design a θh for the heat sink such that the $Tc < 100^{\circ}C$ condition holds when three channels are operating at maximum levels, i.e., $Pd(TOTAL) = Pd(one channel) \times 3$.

 ΔTc will be 100 - 60 = 40 °C, and therefore:

$$\theta h = \Delta Tc \div Pd (TOTAL) = 40 \div (6.8 \times 3) = 2.0$$
, i.e. $\theta h = 2.0$ °C/W

In actual practice, the ambient temperature and operating conditions will allow a heat sink smaller than that indicated by this calculation to be used. Therefore, design optimization taking the actual conditions and the above data into account is also required.





V _{CC} (V)	V _{BB} (V)	V _{OUT} (V)	V _O (center)	
80	10	40	45	

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